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EDN®

EDN's DSP-chip directory

Engineering in Asia: Making it in Taiwan

Troubleshooting analog circuits—Part 11

Universal-input supplies

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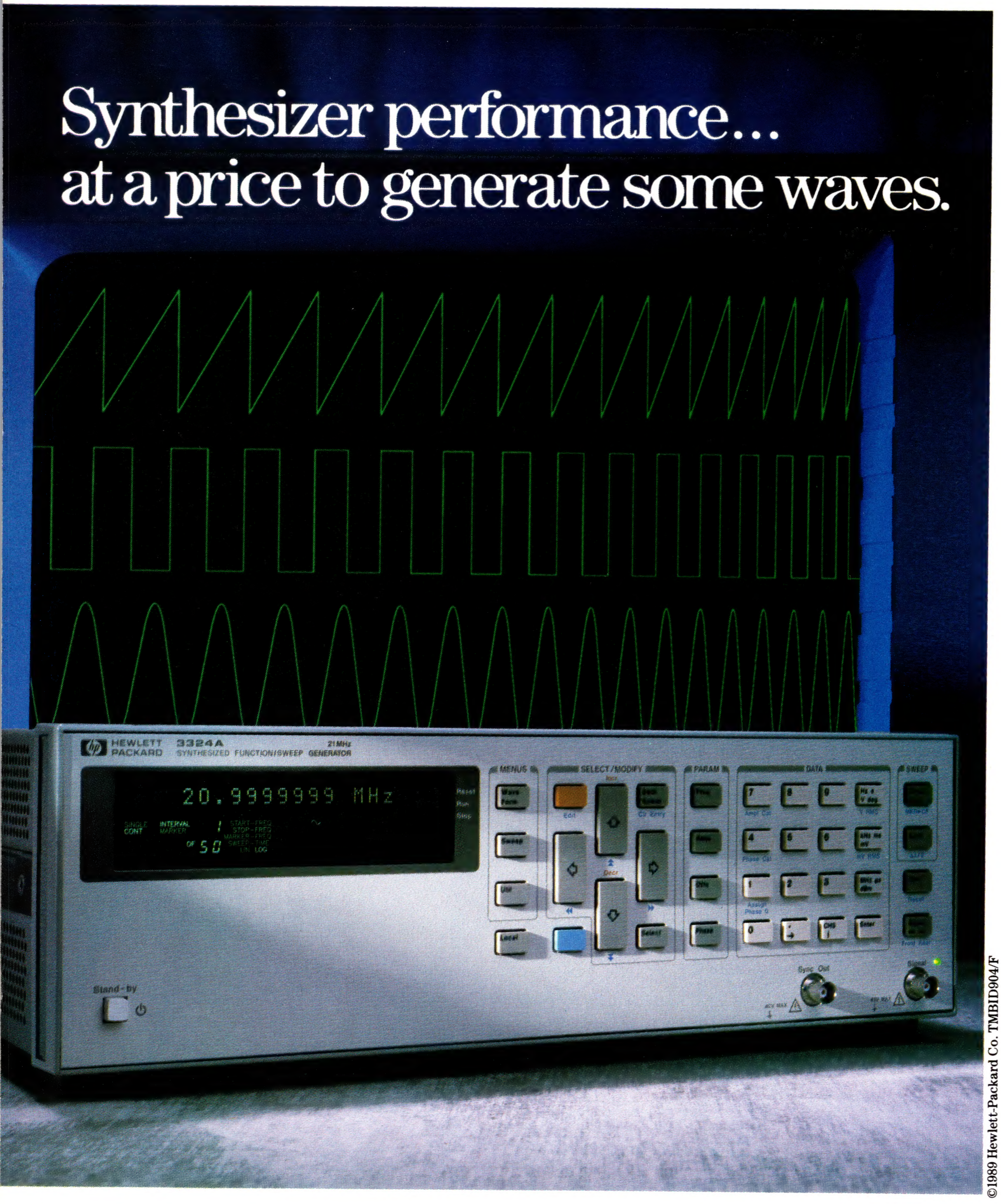

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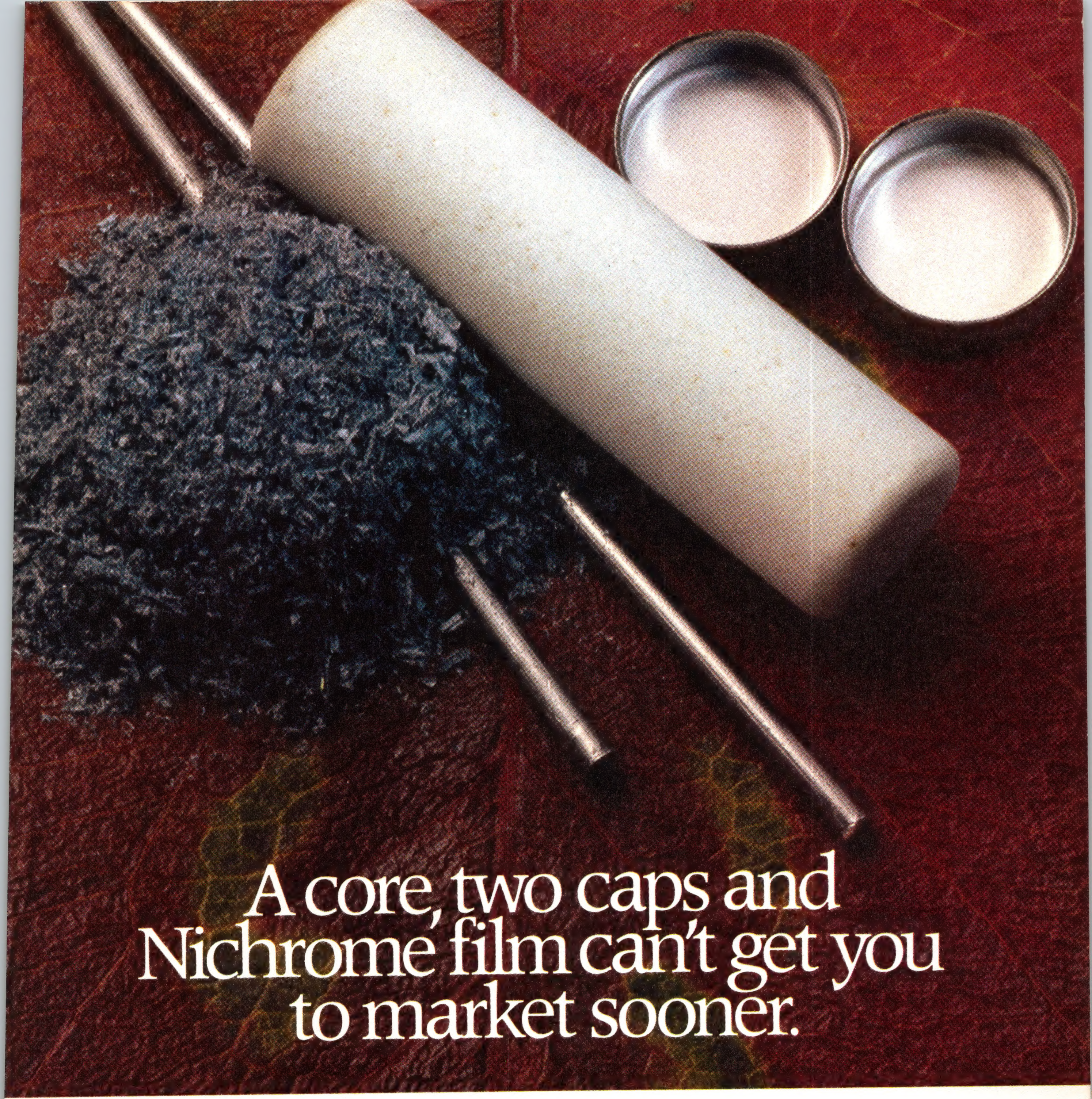
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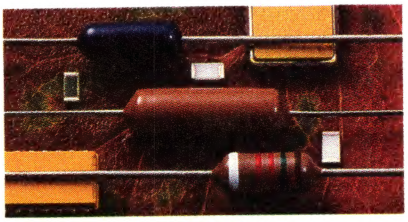

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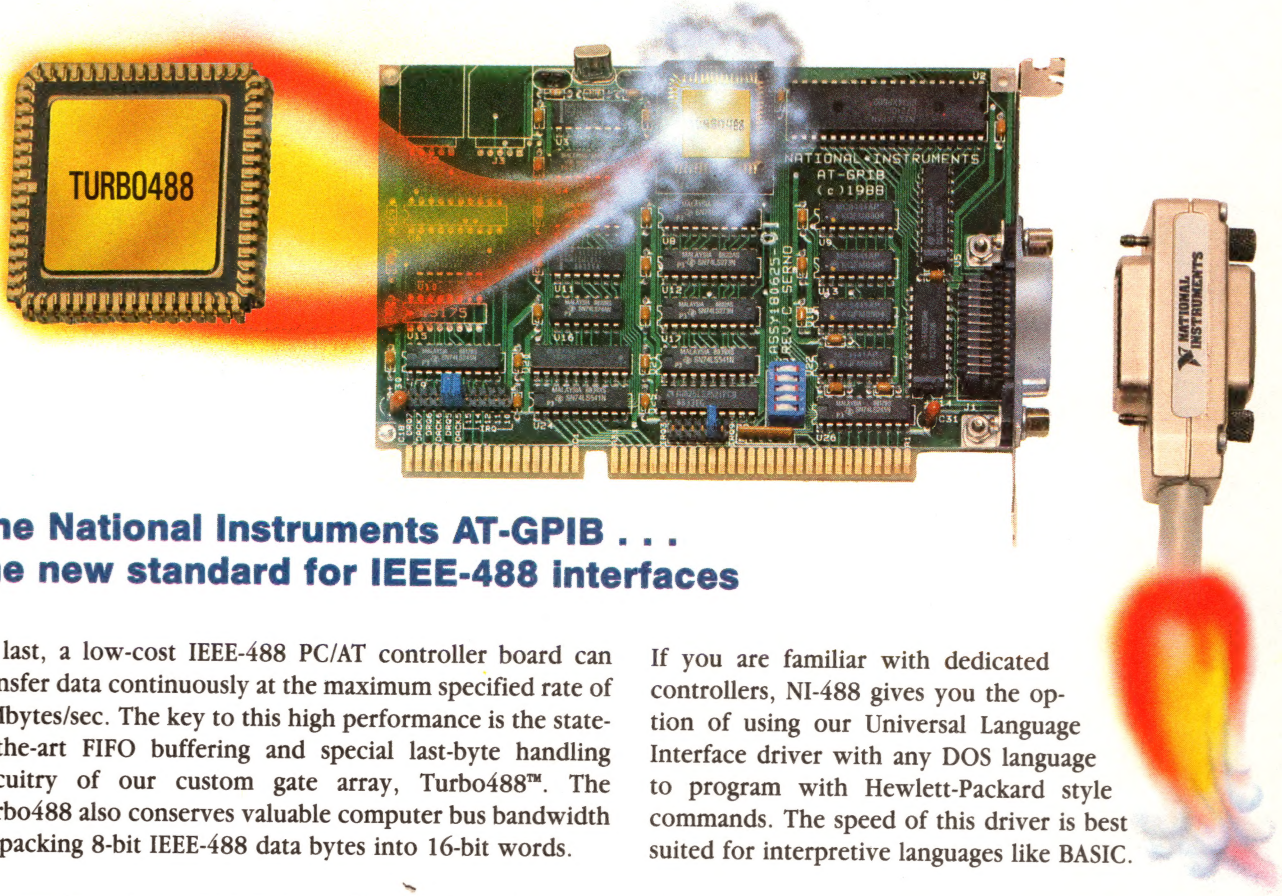

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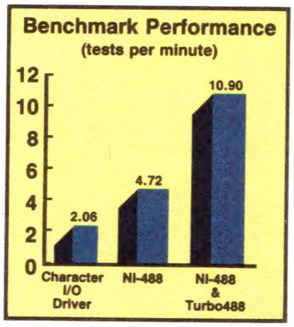

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100-1500MHz	1.1	1.9	1.1	1.7
1500-3000MHz	1.8	2.7	1.8	2.5
Isolation(dB)	typ.	min.	typ.	min.
10-100MHz	60	40	60	40
100-1500MHz	40	28	40	30
1500-3000MHz	35	22	35	22
1dB Compression(dBm)	typ.	min.	typ.	min.
10-100MHz	17	6	17	6
100-1500MHz	27	19	27	19
1500-3000MHz	30	28	30	28
VSWR(ON)	typ. 1.3	max. 1.6	typ. 1.3	max. 1.6
Switching Time (μsec) (from 50% TTL to 90% RF)	typ. 2.0	max. 4.0	typ. 2.0	max. 4.0
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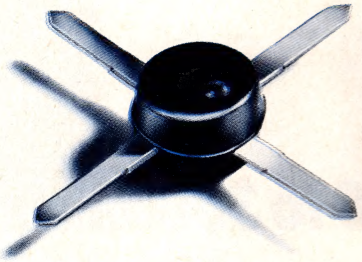

dc to 2000 MHz amplifier series

SPECIFICATIONS

MODEL	FREQ. MHz	GAIN, dB 100 MHz	1000 MHz	2000 MHz	Min. (note)	• MAX. PWR. dBm	NF dB	PRICE Ea.	$ Qty.
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MAR-2	DC-2000	13	12.5	11	8.5	+3	6.5	1.50	(25)
MAR-3	DC-2000	13	12.5	10.5	8.0	+8☐	6.0	1.70	(25)
MAR-4	DC-1000	8.2	8.0	—	7.0	+11	7.0	1.90	(25)
MAR-6	DC-2000	20	16	11	9	0	2.8	1.29	(25)
MAR-7	DC-2000	13.5	12.5	10.5	8.5	+3	5.0	1.90	(25)
MAR-8	DC-1000	33	23	—	19	+10	3.5	2.20	(25)

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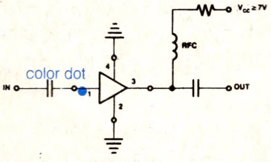

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CIRCLE NO 166

EDN® Magazine Edition

Volume 34, Number 21

October 12, 1989

ELECTRONIC TECHNOLOGY FOR ENGINEERS AND ENGINEERING MANAGERS

On the cover: *Until a few years ago, liquid-crystal displays were relegated to low-performance applications. Improved technologies have drastically changed the application base for these devices. See the Special Report, which begins on pg 102. (Photo courtesy SAI Technology; photography by Kirby N Harris)*

SPECIAL REPORT

Liquid-crystal displays 102

Liquid-crystal displays (LCDs) continue to change the way people view information. From the ubiquitous 7-segment character displays to the large-area displays used in portable computers, LCDs are making a strong bid to dominate the flat-panel-display market.—*Dave Pryce, Associate Editor*

Making it in Taiwan: Life at a Taipei computer company 57

This article is the first in a series that will examine the electronics-engineering profession in Asia. The first installment describes the operation of DTK Computer and the way in which its employees must work.—*Gary Legg, Special Projects Editor*

DESIGN FEATURES

EDN's DSP-chip directory 125

The insatiable demand for speedy, accurate number-crunching capabilities is fostering the development of DSP chips that exhibit supercomputer-like math performance. Both fixed- and floating-point units are reaping the benefits of intense development efforts.—*Bill Travis, Contributing Editor*

Make your surface-mount pc boards testable 143

To achieve higher performance in less space, designers are using surface-mount devices on pc boards that comprise state-of-the-art electronic systems. However, even the most technically elegant and sophisticated surface-mount design is useless—unless you can also test and manufacture it profitably.—*Katherine Gambino and John Kenney III, Valid Logic Systems*

Continued on page 7

BPA ABP

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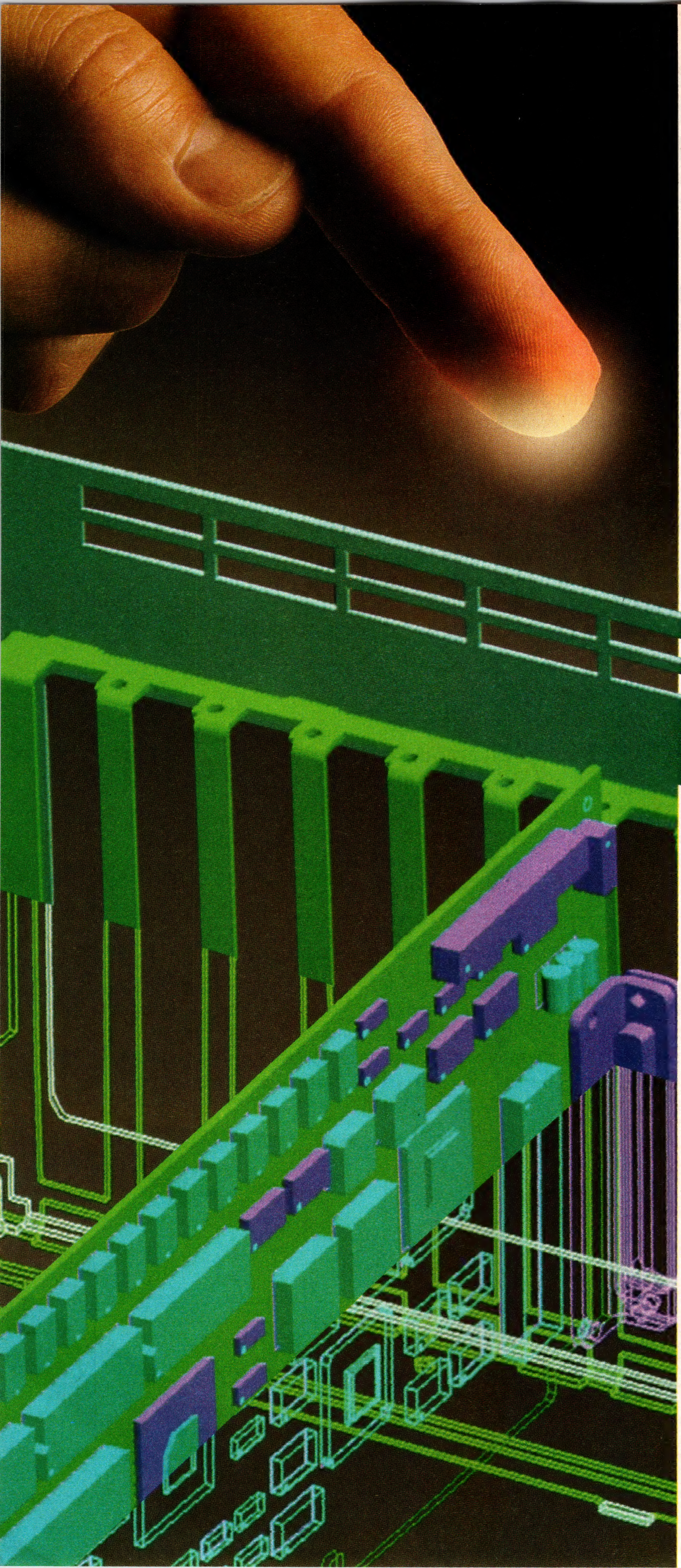

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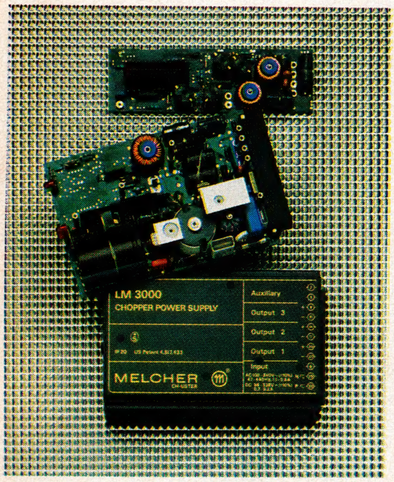

***Several manufacturers** have offered universal-input power supplies that accept inputs ranging from 85 to 265V ac (pg 75).*

Designer's guide to microcontroller simulation: Part 2 — 161

Part 1 of this 2-part article discussed key issues in design-verification testing and presented a simple example of how a simulator can help you test for potential hardware failures. Part 2 presents another, more complex, example of the use of simulation to debug difficult real-time problems.—*Anders Gezelius, Archimedes Software Inc*

Troubleshooting analog circuits Part 11 — 177

Bob Pease—the self-appointed Czar of Band Gaps—continues his series with words of wisdom on voltage references, regulators, and start-up circuits. He also warns against assumptions about worst-case conditions and discusses the usefulness of Kelvin connections. Next time, Bob wraps up this series with some final remarks about troubleshooting.—*Robert A Pease, National Semiconductor Corp*

Interface power MOSFETs to logic devices — 191

Though you can interface today's FETs directly to some logic devices, you must first evaluate such subtle points as low-supply-voltage conditions, power-supply on-off sequencing, and reliability effects of the interface on the logic devices and the FETs.
—*Ken Berringer, Semiconductor Products Sector, Motorola Inc*

TECHNOLOGY UPDATE

Universal-input power supplies: Units suit power needs around the world — 75

To compete in worldwide markets, manufacturers of ac/dc power supplies must ensure that their products accommodate a wide range of inputs. Today's universal-input supplies eliminate, among other things, the possibility of mistakenly supplying 220V ac to a device strapped for 110V ac operation.
—*Tom Ormond, Senior Editor*

Continued on page 9

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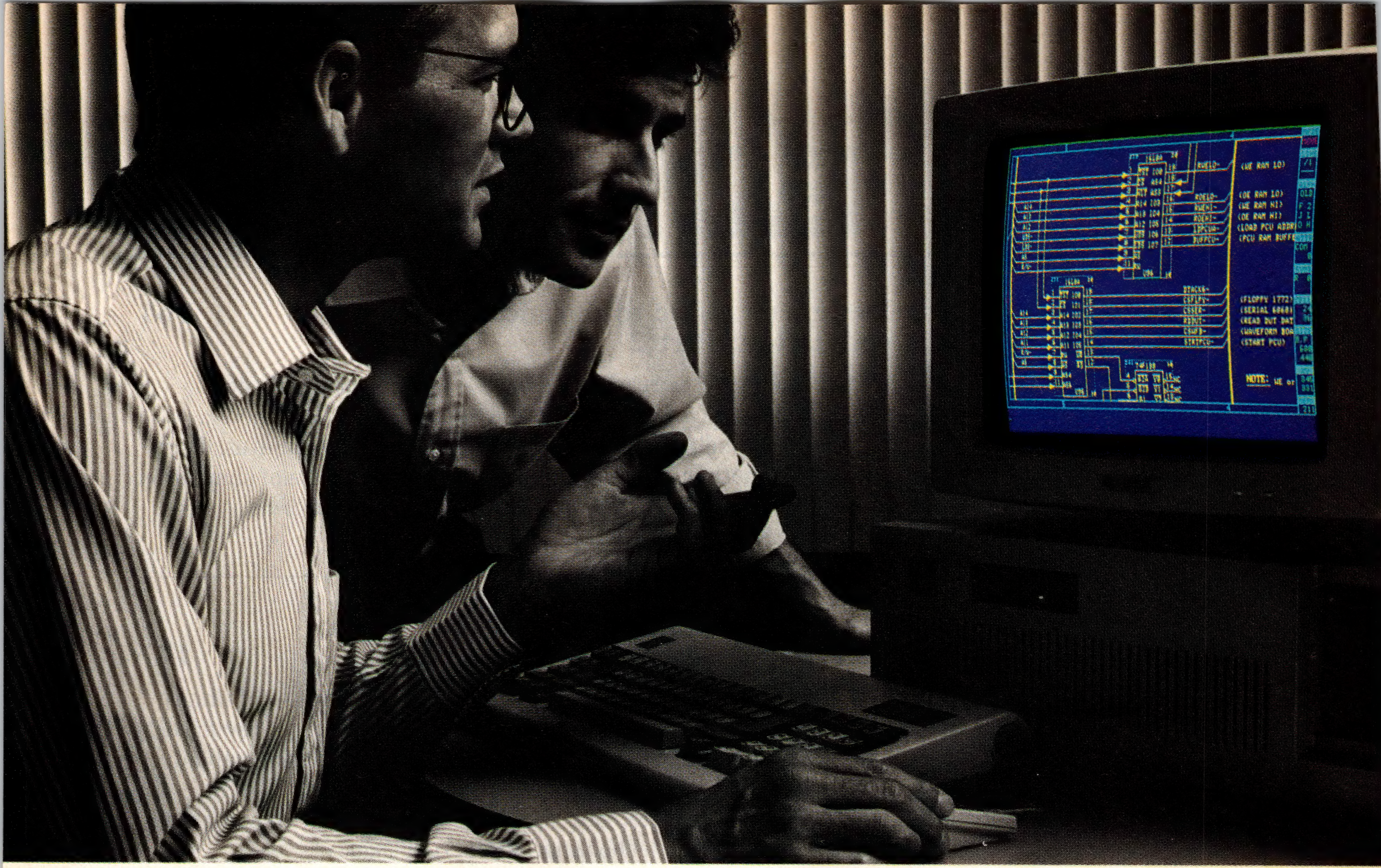

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Things don't always work out, but let's take responsibility for our actions rather than simply covering up with a happy smiley face.

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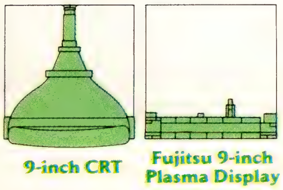

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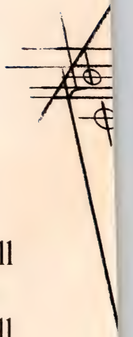

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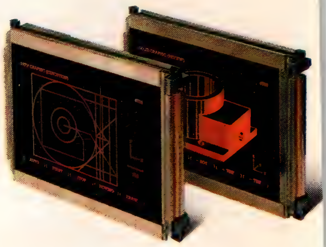

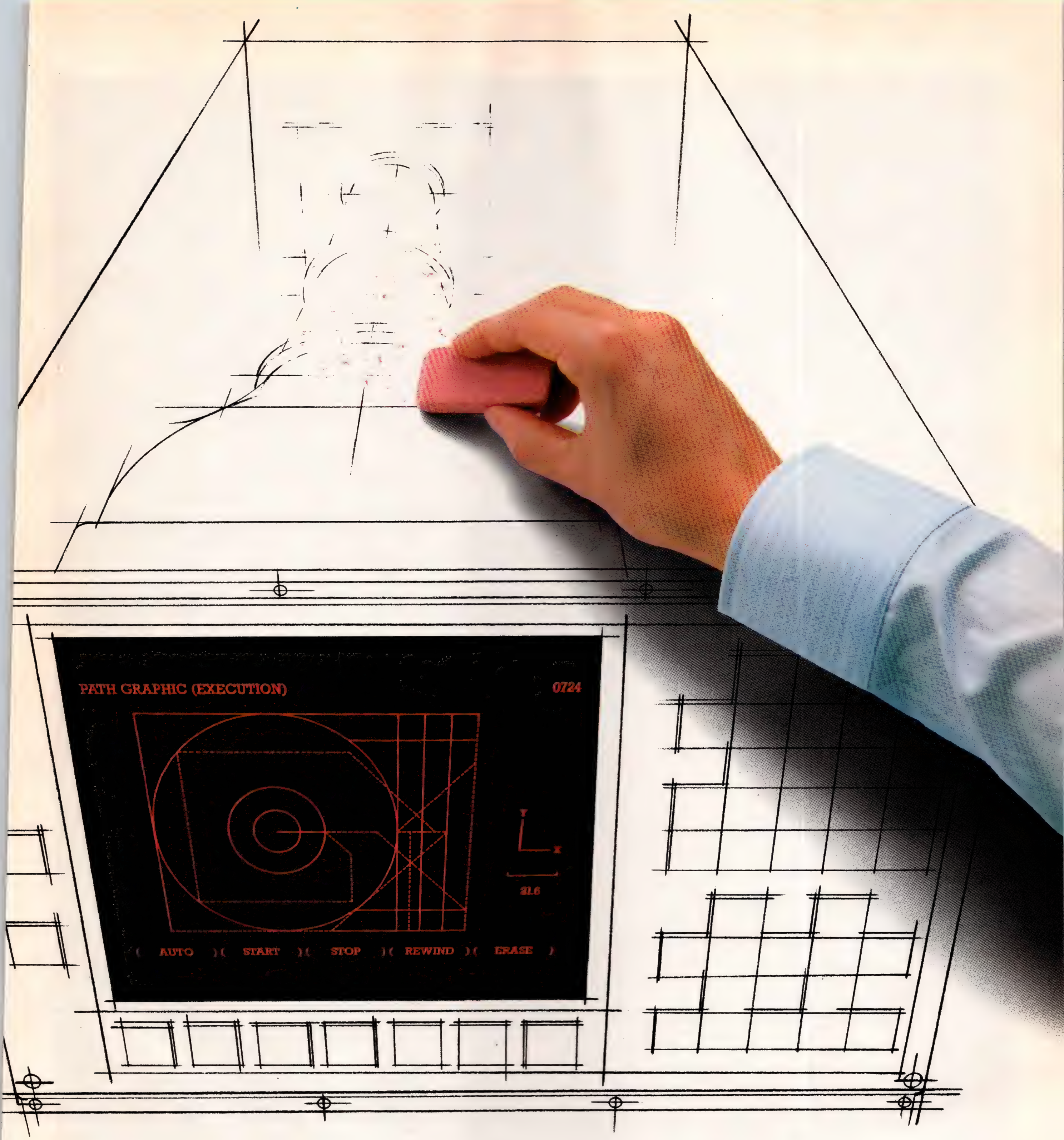

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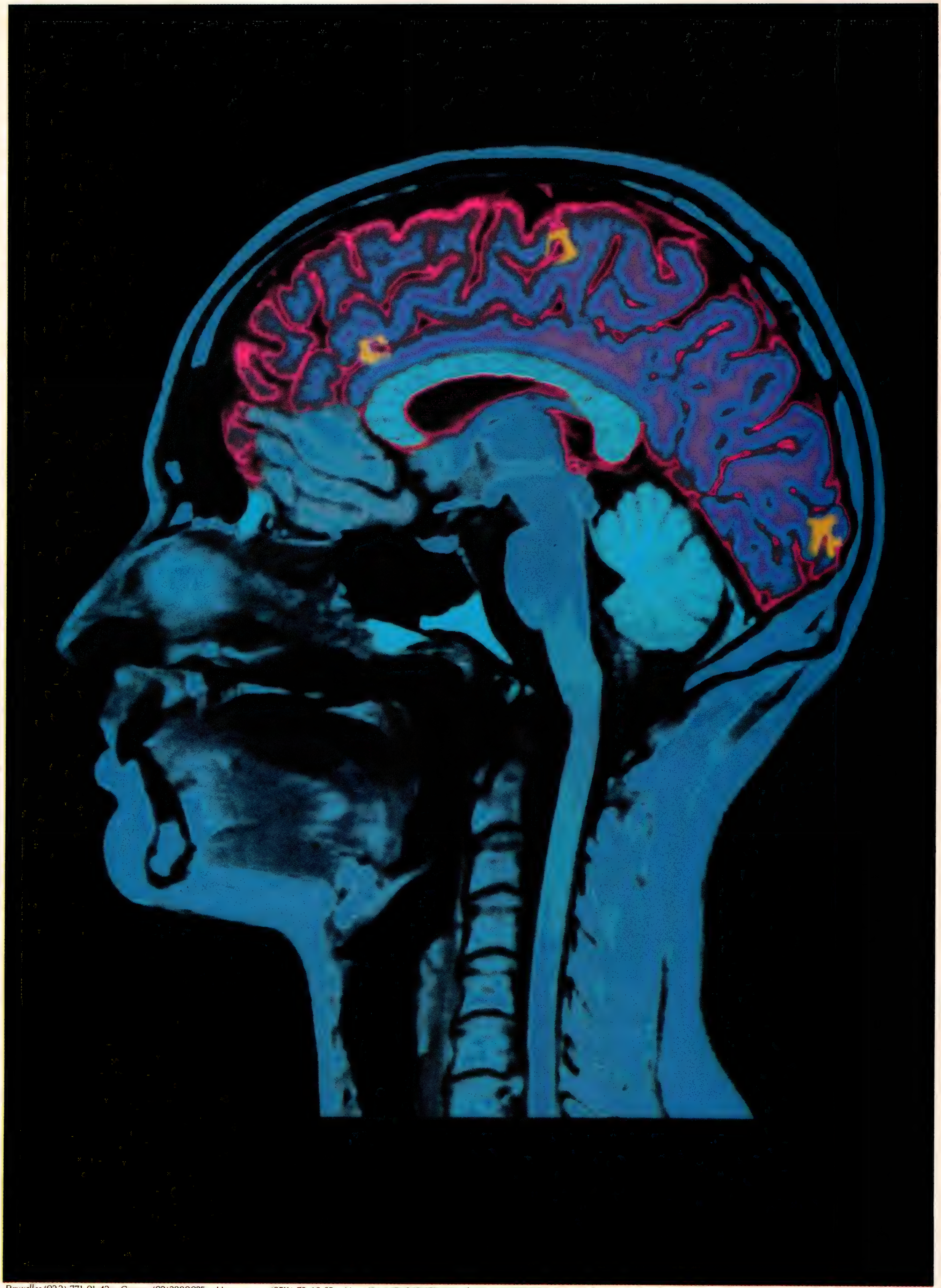
CIRCLE NO 14



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Gates batteries have helped power Physio-Control medical products for more than a decade. That's because, at Gates, we believe in longterm relationships. So, whether you're developing a new product or trying to improve an existing one, we can help you like nobody else.

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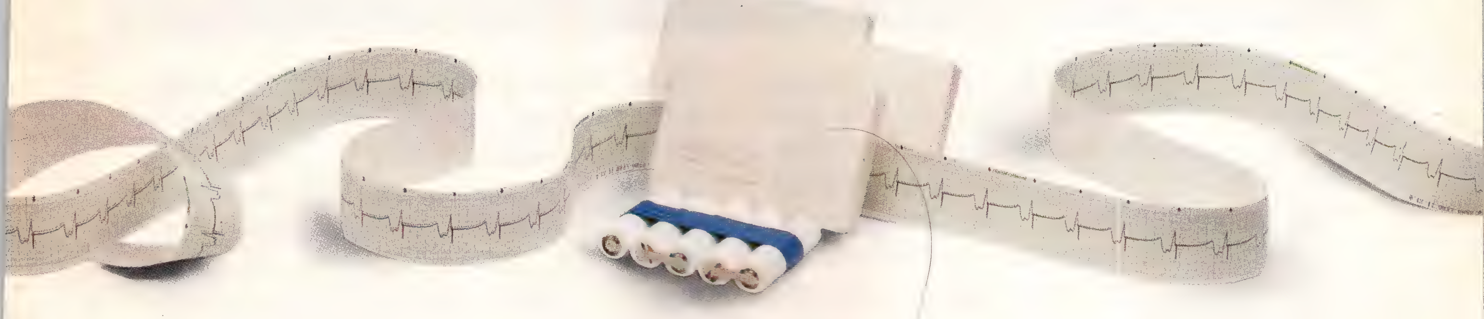
The power that helped it get there.



Qualification Program (ATQP™), advanced new product development to meet specific customer needs.

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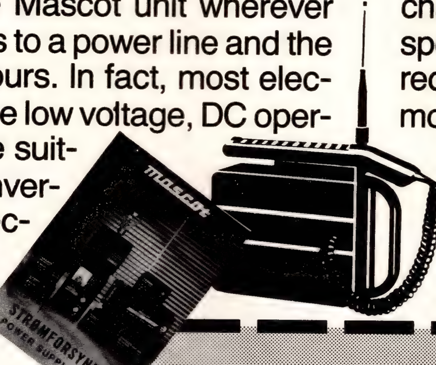
All cellular radios can be used in connection with 110 or 220 V AC. All you need is a small powerful unit that converts AC to 12 V DC. This will extend the use of your cellular radio enormously. Just plug in the Mascot unit wherever you have access to a power line and the connection is yours. In fact, most electronic devices are low voltage, DC operated and require suitable AC/DC converters. Mascot Electronic is Scandinavias' largest manufacturer of power supply units with a complete range of more than 50 models - AC/DC power supplies, DC/DC converters, DC/AC inverters, battery eliminators, chargers..... And even more, customer specified units in small or large series on request. Since 1964 we have delivered more than 4 million power supply units to the leading electronics industry inEurope. So whenever you need reliable power supplies, ask for Mascot.



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The 5-digit, vacuum-fluorescent dual displays give you more information in less time – and with less effort. For example, measure the VDC output of a power supply while measuring the VAC ripple. Or check the amplitude and frequency of an AC signal. From a single test connection!

And the Fluke 45 is designed to make complex measurements easier, with standard features like a 1 MHz frequency counter, Min Max, limits testing (Hi/Lo/Pass), Touch Hold® and Relative modes. There are 21 different reference impedances for dB measurements; in the 2 Ω to 16 Ω ranges, audio power can be automatically displayed in watts.

Accuracy to get the job done right.

The Fluke 45 is a true-rms meter, with 0.02% basic dc voltage accuracy and full 5-digit resolution on both displays. Basic dc current accuracy is 0.05%, making the 45 ideal for servicing 4-20 mA current loops. Closed-case calibration simplifies the calibration process and increases uptime.

Even an RS-232 interface is standard.

Connecting the Fluke 45 to PCs, RS-232 printers and modems is as easy as attaching the cable. An IEEE-488.2 interface and rechargeable batteries are available as options.

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Fluke 45

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That's a big promise, but the 68302 is more than up to it. With three high performance serial communications controllers, each with multiprotocol capabilities, the 68302 can run anything from ISDN, WANs and packet networks to bridges, concentrators, gateways, peripheral I/O, modems and more.

ISDN, by the way, leads that list for a very good reason. Because the 68302's multiprotocol capabilities are the first sensible way to migrate today's proprietary and defacto protocols to emerging standards like ISDN.

RUN ON A POWERFUL 68000 PLATFORM.

The 68302 operates on a 68000-based core and it's fully compatible with the wide world of existing 68000 software. And with our growing 68300 family of microcontrollers.

All that compatibility, obviously, can save you loads of development time and lots of money.

In addition to the 68000-core processor, the 68302 features a powerful, high-speed RISC-based communications processor.

This dual processor approach yields efficient communications processing. Not to mention the highest performance communications controller on the market.

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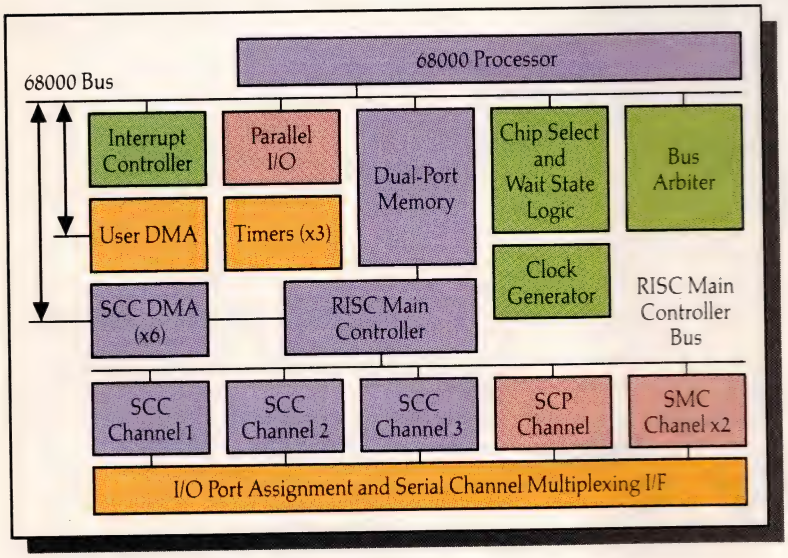
NOW A WORD ABOUT THE ECONOMY.

To save you even more money (and a bit of board space), the 68302 is the most highly integrated communications controller around. In addition to its mighty processors, it comes with a system integration module that's loaded with system glue logic (see diagram for details) you'd otherwise have to provide yourself.



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For more information on the 68302, the third-party support behind it, and our 68302 Application Development Systems Evaluation Board, call 1-800-441-2447. Or contact the Motorola Semiconductor sales office nearest you.

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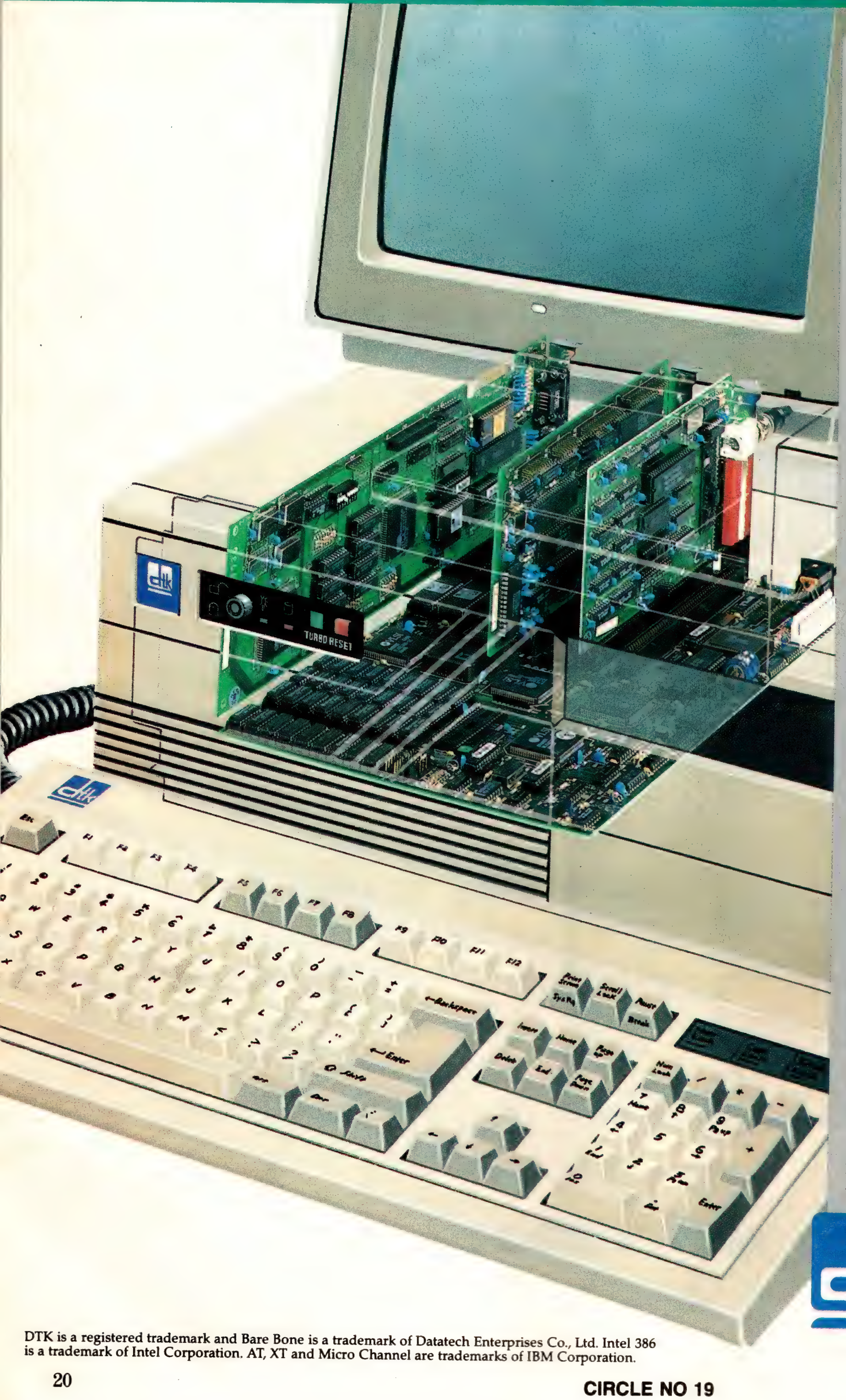

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CIRCLE NO 19

NEWS BREAKS

EDITED BY JULIE ANNE SCHOFIELD

LOGIC ANALYZER'S TRIGGERING ECHOES YOUR THOUGHT PATTERNS

The Prism 3001HSM hardware-analysis logic analyzer is the newest member of Tektronix Inc's (Portland, OR, (800) 426-2200) recently introduced Prism 3000 family. By using a group of "leadsets," units commonly known as pods, you can tailor the 3001HSM's capabilities to your needs. The instrument also lets you establish trigger conditions based on the way you think about hardware problems. For example, the analyzer will trigger directly on setup times that violate limits you specify or on pulse durations narrower than a value you supply. All told, the unit performs 15 fault-condition tests.

With the appropriate leadsets, the analyzer can acquire data asynchronously at 2 GHz or perform 20-channel timing analysis at 400 MHz. In the latter mode, the instrument uses transitional timing to effectively increase its memory depth beyond 12k words. The unit can acquire data synchronously at 300 MHz—200 MHz when performing dual-threshold acquisition, a technique useful for spotting marginal amplitude conditions. You can also add a leadset that digitizes analog waveforms to 11 levels (3½ bits) at 400M samples/sec. The heart of the analyzer is a large pc card, the 30HSM. Ten 30HSMs can plug into Tektronix's Prism 3002 series units. The 30HSM costs $6500; the 3001HSM—a complete, self-contained instrument—carries a base price of $11,000.—Dan Strassberg

CAD VENDOR GIVES SOFTWARE TO SCHOOLS

To give students familiarity with computer-aided-engineering, computer-aided-design, and computer-aided-manufacturing (CAE/CAD/CAM) software, Design Computation Inc (Farmingdale, NJ, (201) 938-6661) is offering versions of its software to qualified IEEE-affiliated schools through CADET (Staten Island, NY, (718) 442-1053), a value-added reseller specializing in CAE, CAD, and CAM. The package, DC/CAD-Classroom, is a doctored version of the vendor's DC/CAD package that comes with no copy protection and supports small- to medium-sized designs. DC/CAD-Classroom includes schematic capture, a pc-board layout tool with interactive and automatic parts placement, and interactive routing. Qualified schools receive the manuals and training materials, and Design Computation encourages students to make and distribute copies for their own use. This offering supplements the vendor's earlier release of a classroom version of its DC/Design interactive routing package. For nonqualified users, the software costs $1395 for DC/Design and $3495 for DC/CAD.
—Michael C Markowitz

NEW SOURCE FOR AUDIO A/D CONVERTER

A high-resolution A/D converter chip set originally developed by dbx is now available to American and European customers from UltraAnalog Inc (Fremont, CA, (415) 657-2227). Carillon Technology (Sunnyvale, CA, (408) 720-9800), the parent company of dbx, will continue to offer the ICs to Far East customers. The chip set is based on a delta-sigma algorithm and includes the F410 front-end IC, the D20C10 decimator IC, and the A1520 precision-resistor array. The A/D converter can achieve 18 to 20 bits of resolution for standard digital-audio sampling rates of 32, 44.1, and 48 kHz, and depending on the configuration you use, the SNR can reach 114 dB. For a typical 18-bit design, the chip set costs $130 (100).—Anne Watson Swager

NEWS BREAKS

CONSORTIUM TO OFFER FRAMEWORK TEST SUITE

In an effort to serve as an independent proving ground for CAD frameworks, the Microelectronics and Computer Technology Corp (MCC) (Austin, TX, (512) 343-0978) is working to develop the CAD Framework Laboratory (CFL). The CFL's objective will be to support the standards that the CAD Framework Initiative (CFI) (Boulder, CO, (303) 530-4562) proposes and adopts. The CFI is an industry effort to promote the standardization of the interfaces between CAD tools.

Unlike previous MCC efforts, the CAD Framework Laboratory will be available to shareholders and nonshareholders via two levels of participation. Level 1 affiliates will be active participants in the lab and will receive multiple copies of the software verification and validation systems that the lab develops. In addition, one representative from each Level 1 affiliate company may sit on the CFL's Technical Coordinating Committee to resolve technical issues, determine priorities, and provide recommendations to CFI. Level 2 affiliates can attend meetings but do not have voting rights. They do, however, have access to a single-machine copy of verification and validation software. MCC hopes that the CAD Framework Laboratory can serve as medium for speeding the evaluation and exchange of comments between the users and the CAD Framework Initiative.—Michael C Markowitz

V.32 MODEM MODULE SUPPORTS 12,000-BPS OPERATING MODE

At the TCA show in San Diego, Rockwell International (Newport Beach, CA, (714) 833-4700) introduced the RC9696/12 V.32 modem, which includes a 12k-bps turbo mode. The module measures approximately 3¼×4 in. and fully supports the 9600-bps V.32 standard for dial-up operation over the public switched-telephone network. The RC9696/12 also offers downward compatibility with industry-standard 7200-, 4800-, 2400-, 1200-, 600-, and 300-bps modems. The product designers employed a trellis-coded-modulation scheme to improve error detection and correction in the V.32 mode and the proprietary 12k-bps mode. Shipments will begin in November for the $250 (1000) modem.—Maury Wright

LOGIC ANALYZER OFFERS DISASSEMBLER FOR THE 80960CA

Designers using the Intel 80960CA processor now have available a logic analyzer that can disassemble the 960CA's instructions if the cache is disabled. The Fluke (Everett, WA, (206) 347-6100) PM 3655R is an IBM PC-compatible, 100-MHz, 96-channel logic analyzer with 2k bytes of memory per channel and a hard-disk drive. The disassembler operates under MS-DOS and offers 12 trigger words with four levels of IF-THEN-ELSE triggering. You can handle nested translation tables, use symbolic labeling, and set up area traces that allow selective data recording. The unit costs $13,200.—Richard A Quinnell

PC-BASED SCHEMATIC-CAPTURE PROGRAM COSTS $295

Shooting for the low-cost end of the schematic-capture market, Phase Three Logic Inc (Beaverton, OR, (503) 645-0313) has just introduced its $295 CF640 software package, which requires only 640k bytes of RAM yet supports hierarchical schematics that span several pages and include as many as 10,000 components. The company achieves this capacity through memory overlays. You can run the CF640 package

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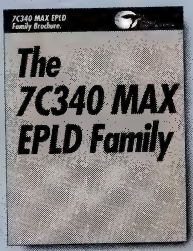

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on all IBM PCs, PS/2s, and compatible machines with EGA or VGA display adapters, but the vendor recommends that your computer have an 80286 or 80386 µP to obtain reasonable response times. You'll also need 12M bytes of space on your hard disk to run the program. In addition to the schematic-capture program, the package includes a components library containing more than 5500 parts, a parts-list generator, simulation interfaces, PLD compiler interfaces, interfaces to several pc-board-layout packages, and one year of software support.—Steven H Leibson

BICMOS ECL I/O SRAM FAMILY GAINS NEW MEMBERS

National Semiconductor (Santa Clara, CA, (206) 841-6666) has enhanced its BiCMOS-based ECL I/O static-RAM (SRAM) family by adding 16k × 4- and 64k × 4-bit configurations. Both devices are available in a variety of speed grades in both DIP and flatpack packages. You can get the NM10494 16k × 4-bit, 10K ECL SRAM with access times of 10, 12, or 15 nsec; the NM100494 100K version has an access time of 15 nsec. The NM5104 operates with $V_{EE} = -5.2V$ but offers a 100K ECL interface; it comes in 12, 15, and 18 nsec speeds. The NM100504 operates as a standard 100K device with speed grades of 15 or 18 nsec.

The pinout of the 64k × 4-bit flatpack devices is identical to that of the 16k × 4-bit devices, thus you can design a memory board that can be upgraded without additional engineering. The 64k × 4-bit DIP pinout is a straightforward extension of the JEDEC standard pinout for 16k × 4-bit devices. The 64k × 4-bit, 12-nsec parts cost $175 (100); the 16k × 4-bit, 10-nsec parts cost $115 (100).—Richard A Quinnell

2½-in. HARD-DISK DRIVE STORES 42.8M BYTES

Targeted at laptop computers and other portable applications, the diminutive Prairie 240 hard-disk drive from PrairieTek Corp (Longmont, CO, (303) 772-4011) stores 42.8M bytes (formatted) yet measures only 1 × 2.8 × 4.8 in. In addition to its small size, the drive consumes a small amount of power: an average of less than 1.5W while running. An automatic mechanism parks the read/write heads when you remove power. The parking mechanism actually lifts the heads from the magnetic media so the drive can withstand the severe shocks that portable equipment must often endure. The Prairie 240 incorporates an integrated IBM PC AT/XT disk controller, weighs 9 oz, and has an average access-time rating of 28 msec. Evaluation units cost $750.—Steven H Leibson

PACKAGING SCHEME EASES LIGHT PASSAGE TO PHOTODETECTOR

You can easily connect a fiber-optic cable from a remote sensor to the SD-225-23-21-040 quadrant photodetector from Silicon Detector (Camarillo, CA, (805) 484-2884). The $18 detector has a laser-drilled light-source hole through the back of its detector chip and TO-8 package header. This scheme lets the fiber-optic cable get to within 0.003 in. of the sensor's active area, which is on the top of the chip. Dark currents per element are 2.8 nA or less at 10V with a shunt resistance of at least 5 00 MΩ.
—Margery Conner

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MODEL	FREQ. RANGE (MHz) f_L to f_u	GAIN dB min	flatness††	MAX. OUT/PWR† dBm	NF dB (typ)	DC PWR 12V, mA	PRICE $ ea. (10-24)
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MAN-1LN	0.5-500	28	1.0	8	2.8	60	15.95
◇MAN-1HLN	10-500	10	0.8	15	3.7	70	15.95
*MAN-1AD	5.500	16	0.5	6	7.2	85	24.95

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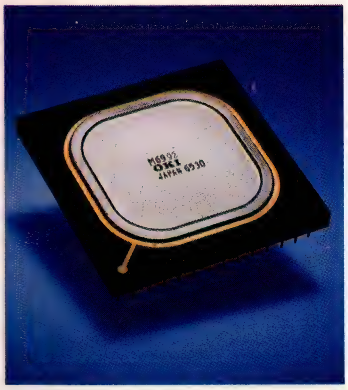

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CIRCLE NO 29

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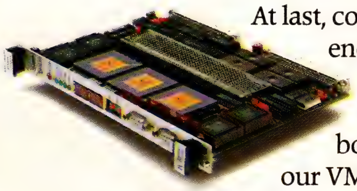

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Again.
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Rats.
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CIRCLE NO 31

SIGNALS & NOISE

Clearing up a misunderstanding

The News Breaks item "Power-factor corrector boosts power utilization" (EDN, June 22, 1989, pg 23) contains a misunderstanding. The cause of low power factor in switch-mode power supplies is not the phase of the current waveform. Low power factor is a phenomenon common to inductive loads such as ac motors, and you can correct it by adding a parallel capacitor to the load.

The problem with a traditional power supply is that the current waveform is a very narrow pulse. You can obtain more power for a given rms current (which is limited by the ac supply) when the current waveform is a sinusoid. The device as described, as well as some other devices, draws a near-sinusoidal current from the ac line and provides the power to the power-supply circuit.

Carl Spearow
Senior Engineer
Sundstrand Corp
Rockford, IL

Contributions of the "few" should be compensated

The editorial [by Jon Titus] advising rejection of patent protection for mathematical/algorithmic work (EDN, April 27, 1989, pg 45) identifies a very interesting problem whose ultimate solution is obviously headed in a direction opposite to Jon Titus's desires.

It is unthinkable to continue to allow the fruits of the labor of creative people in the mathematical and physical sciences to be the uncompensated basis for the generation of so much of the world's economic well being. A vast amount of human progress is based on "intellectually" derived contributions by a few people, be it quantum mechanics or Fourier transforms. And, although traditional perceptions of what constitutes the highest human ideals would make abhorrent the goal of financial enrichment from intellectual endeavors, it is also true that "Mozart dying in poverty" has an equally repulsive sound.

In a more pragmatic bottom-line sense, it should be noted that the protection of "mental exercises" would have made the trade deficit with Japan nonexistent if one considers as true the common perception that they simply added "quality control" to "ideas" created elsewhere.

Tasso Politopoulos
Ford Aerospace Corp
Newport Beach, CA

Engineers as a commodity in the work market

In reponse to the letter, "Non-US engineers benefit the industry," (EDN, July 20, 1989, pg 35,) [I'd like to repeat the] fable I read as a child about five blind men who happened on an elephant. Each blind man encountered a different part of the elephant. Upon learning it was an elephant, one man who felt the elephant's trunk concluded that the elephant was like a snake, and another man who encountered a leg thought the elephant was like a tree. Each man developed a different impression of the entire elephant, depending on what part he was holding onto.

Engineers shouldn't make the same mistakes as the five blind men. They owe it to their profession to open their eyes to all issues confronting engineers in working careers. The product cycle usually begins with the systems engineers who develop the product concept. These engineering teams are usually small in number, and their ranks are composed of engineers with specialized skills. As the product goes to the design/prototype/test stage, a larger number of engineers is needed. The manufacturing

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CIRCLE NO 32

stage employs support engineers where the bulk of engineers is concentrated. [Therefore,] one cannot extrapolate the experiences of any one group and claim that a particular group's experience is representative of the entire engineering spectrum.

Engineers have also been debating over terms that have different definitions. Two of these divisive terms are "professional" and "shortage." The term "professional" conjures up a picture of a dedicated entrepreneur in the engineer's mind, in the mold of a private-practice doctor or lawyer. In the minds of the business community, the engineers are laborers whose salaries affect the company's bottom-line profits. To the business community, the term "professional" means "exempt," which, in turn, has a bottom-line currency value meaning that engineering overtime does not have to be paid.

The term "shortage" also suffers from dual-definition syndrome. The engineer and most of the lay community think that "shortage" means there is a broad-spectrum shortage of engineers, and that the business community can use every engineer they can lay their hands on, regardless of age or other attributes. To the business community, "shortage" means that there are not enough engineers in the right price or age range. Engineering labor prices affect the profit picture, especially as an engineer gets older. Several things happen that affect the corporate profit picture: 1) There's an increase in salary; 2) there may be a larger impact on the engineer's medical benefits; and 3) the engineer approaches pension age. The business community constantly seeks to restructure its labor portfolio to increase profits by all means necessary.

During this last decade the business community has been preoccupied with productivity, which has been enhanced mainly through personnel reduction spawned by the advent of automation tools. Productivity increases have come about by integrating the remaining personnel into an automated environment. [This practice] usually means that the company can do the same amount of work with fewer people in [either] a shrinking or an expanding market. The engineering community has also felt the impact of these automation tools.

Engineers should be united in supporting goals that will improve the engineers' quality of life in the workplace. We should not waste time debating with each other over our misconceptions of labels because [dissension among ourselves] only promotes the divide-and-conquer goals of other interests. While we divisively debate esoterica, the engineering profession is drained of the focus and energy needed to pursue the betterment of our workplace and the safeguarding of our career investments.

Jim Glendenning
Long Beach, CA

PC-controlled instruments are "alive and well" in US

Bill Steckowich's letter (EDN, August 3, 1989, pg 34) dismissing PC-controlled instruments as a "dead horse" proves that backward thinking is alive and well in America. The first attempts to sell personal computers by companies like Viatron and Umtech were also a flop, but fortunately that didn't discourage Steve Jobs from trying again with Apple Computer.

Here's a news flash for Bill: PCs no longer cost $5000, and vacuum-tube voltmeters have been obsolete for decades. PC prices have already crossed the $1000 mark and will continue to fall rapidly. As a member of the team that designed the Orion OmniLab, I can tell you that "I have seen the future and it works." Using a PC to control integrated general-purpose instrumentation hardware saves significant money, space, and time.

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The exciting thing about the electronics business is that the ground rules are continually changing. Innovation comes when we look into the future and rethink our old assumptions.

Tom Blakeslee
Vice President R&D
Orion Instruments Inc
Redwood City, CA

Another concept of a patent's purpose

My reason for writing is to encourage any misgivings you may have acquired concerning patent law (see Jon Titus's editorial, EDN, April 27, 1989, pg 45.)

I have come to believe very strongly that patent law, at least as it is presently constituted, is an *anachronism*. The argument is that it "protects the little guy from the big guy."[However] I think it is obvious, to one who thinks about it, that it really protects the big guy from the little guy, and that it also inhibits industrial progress. I also wonder if patent law wasn't established during the last century for the de facto purpose of protecting established manufacturers from upstart immigrant competition to facilitate an open immigration policy. For example, I would be an immigrant to whom you, an established manufacturer, were kind enough to give a job. I would learn your manufacturing skills in a few years and

Text continued on pg 37

then quit working for you to become your competitor, copying everything you did. The establishment of patent law coincides with the massive immigrations that began prior to the Civil War.

It is argued that inventors need the incentive of public reward, which is what patent law accomplishes, offering the inventor a monopoly from which he may become rich. Why couldn't patent law be restructured so that inventors are rewarded on the basis of the fact that people have found [the inventors'] inventions good enough to copy, and on the basis of the extent to which they are copied, rather than forbidding their being copied? Everyone in manufacturing should conform to the best, which is what would happen if the monopoly aspect of patent law were removed.

It is also argued, it seems, that the benefits of uniformity in manufacturing would be lost if it weren't for monopoly. I think that that is what "standardized specifications" are for, such as those that might be published by organizations like the IEEE. To be marketable, one's product would have to meet the "specs."

Mark Goodell
Engineering Office
Fort Lee, VA

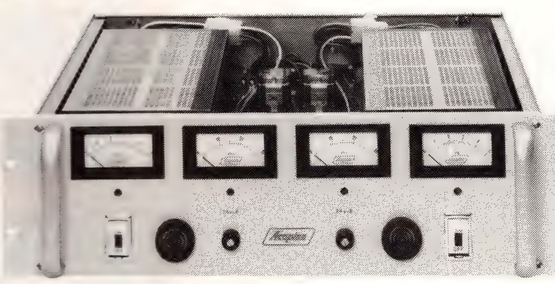
A different kind of relay

In Margery Conner's article (EDN, August 17, 1989, pg 60), she states that the M33C relay can dissipate 486W without a heat sink. A 0.8×1.4×0.25-in. package of anything that dissipates 486W will glow within seconds and is probably better suited for a toaster element.

I believe that the 486W figure is applicable instead to the load-carrying capacity of the relay.

Istvan Mohos
HHB Systems
Mahwah, NJ

REDUNDANT DC POWER



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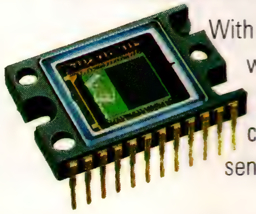

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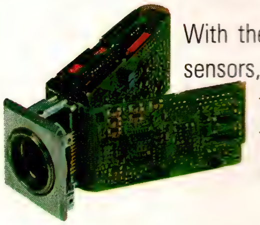

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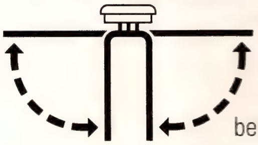

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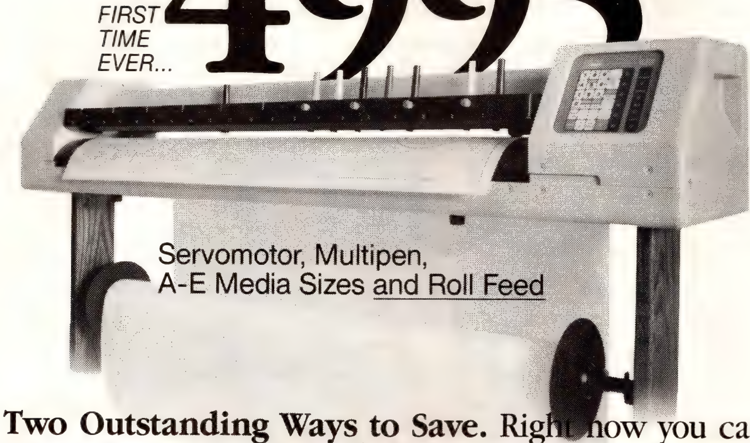

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Policy and Parity: The Future of US-Japan High Technology Trade Policy (symposium), Boston, MA. Janet Fannon, Clearpoint Research Corp, 99 South St, Hopkinton, MA 01748. (617) 435-2301. October 12 to 14.

SECS Communications Seminar, San Jose, CA. GW Associates Inc, 1183 Bordeaux Dr, Suite 27, Sunnyvale, CA 94089. (408) 745-1844. FAX 408-745-6395. October 13.

1989 Linear Applications Seminar, Bellevue, WA. Various locations and dates. National Semiconductor, Box 58090, Santa Clara, CA 95052. (800) 548-4529. Beginning October 16.

Systems 89, Munich, West Germany. Gerald G Kallman, Kallman Associates, 5 Maple Ct, Ridgewood, NJ 07450. (201) 652-7070. FAX 201-652-3898. October 16 to 20.

Northcon/89, Portland, OR. Northcon/89, 8110 Airport Blvd, Los Angeles, CA 90045. (213) 772-2965. October 17 to 19.

Scan-Tech '89, San Jose, CA. Jane Yallum, AIM USA, 1326 Freeport Rd, Pittsburgh, PA 15238. (800) 338-0206. FAX 412-963-8753. October 17 to 19.

Supercomputing World, San Francisco, CA. MG Expositions Group, 1050 Commonwealth Ave, Boston, MA 02215. (800) 223-7126; in MA, (617) 232-3976. October 18 to 20.

The Third Conference on Crystal Growth—The American Association of Crystal Growth, Eastern Region, Atlantic City, NJ. Ed Porbansky, Allied-Signal Inc, Box 1021R, CTC-1, Morristown, NJ 07962. (201) 455-6879. October 18 to 20.

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It was a problem grounded in the laws of electrical energy. And it could have caused real havoc. But the customer took the smart step of calling Dialight.

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CIRCLE NO 101

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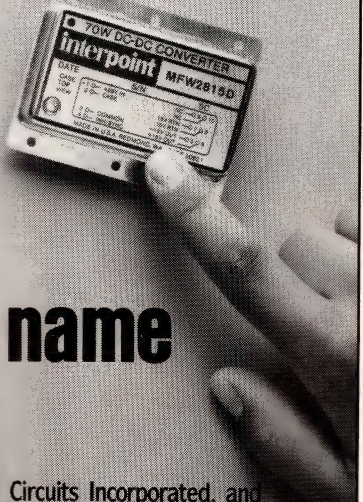
Software Tools for Calculating Minds **#13**

CIRCLE NO 169

We'd like to point out our new MFW Series DC-DC converters...



- Input voltage range 16-40 volts, continuous
- Single, dual, and triple output configurations
- Up to 70 watts of output power
- Power density of 27 watts/cubic inch
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CIRCLE NO 42

CALENDAR

Digital Signal Processing, Single-Chip DSP Processors, Development Systems—Theory, Design and Applications, Munich, West Germany, October 23 to 26; in London, UK, October 30 to November 2. In the US, Dr Amnon Aliphas, DSP Associates, 18 Peregrine Rd, Newton, MA 02159. (617) 964-3817. FAX 617-969-6689. In Europe, Andreas Kohl, Electronic Tools, Dusseldorf, West Germany. (49) 02102-841-013.

1989 DOD-STD 2167A/2168 Seminar, Washington, DC. David Maibor Associates Inc, Box 846, Needham Heights, MA 02194. (617) 449-6554. October 26 to 27.

System Application Architecture (SAA) World (conference and exhibition), Chicago, IL. Digital Consulting Inc, 6 Windsor St, Andover, MA 01810. (508) 470-3880. FAX 508-470-0526. October 30 to November 1.

Unix Expo '89, New York, NY. National Expositions Co, 15 W 39th St, New York, NY 10018. (212) 391-9111. FAX 212-819-0755. November 1 to 3.

Visual Communications and Image Processing '89, Philadelphia, PA. The International Society for Optical Engineering, Box 10, Bellingham, WA 98227. (206) 676-3290. FAX 206-647-1445. November 5 to 10.

OEM Europe '89, Paris, France. Bureau International de Relations Publiques, Freddy J Rodriguez, 25 rue d'Astorg, 75008 Paris, France. (331) 47-42-20-21. FAX 331-47-42-75-68. November 7 to 10.

Fallcon '89, Cedar Rapids, IA. Fallcon '89, Box 451, Marion, IA 52302. (319) 396-7924. November 8 to 9.

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SWITCHING POWER SUPPLIES

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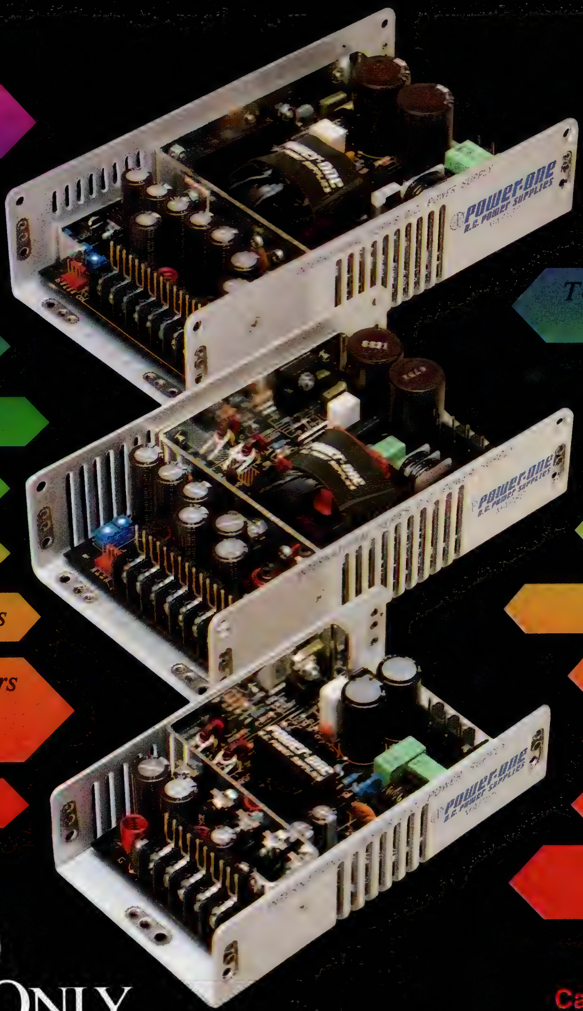
- *EMI Tested to FCC 20780 Class B & VDE 0871 Class B*
- *Less Than 500 μA Leakage Current*
- *Rugged Wrap-Around Chassis*
- *Thermal Shutdown with Warning*
- *Platinum Barrier Schottky Rectifiers*
- *Universal Terminal Block Connectors Include Both Locking Wafer Style Connectors & 6-32 Wire Clamps*
- *75% Typical Efficiency*



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- *Outstanding Application Flexibility*
- *100% Test, Inspection & Burn-In*
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- *3750 VRMS Isolation Plus VDE Safety Spacings*

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MODEL	POWER	OUTPUT 1	OUTPUT 2	OUTPUT 3	OUTPUT 4
MAP55-4000	55W/65W PK	5V @ 6A	12V @ 3A/4A PK	– 12V @ 1A	– 5V @ 1A
MAP55-4001		5V @ 6A	12V @ 1A	– 12V @ 1A	24V @ 1.5A
MAP55-4002		5V @ 6A	12V @ 3A/4A PK	12V @ 1A	– 12V @ 1A
MAP80-4000	80W/110W PK	5V @ 14A	12V @ 4A/7A PK	– 12V @ 1A	– 5V @ 1A
MAP80-4001		5V @ 14A	12V @ 1A	– 12V @ 1A	24V @ 2A
MAP80-4002		5V @ 14A	12V @ 4A/7A PK	12V @ 1A	– 12V @ 1A
MAP130-4000	130W/165W PK	5V @ 20A	12V @ 5A/8A PK	– 12V @ 1A	– 5V @ 1A
MAP130-4001		5V @ 20A	12V @ 1A	– 12V @ 1A	24V @ 3.5A
MAP130-4002		5V @ 20A	12V @ 5A/8A PK	12V @ 1A	– 12V @ 1A

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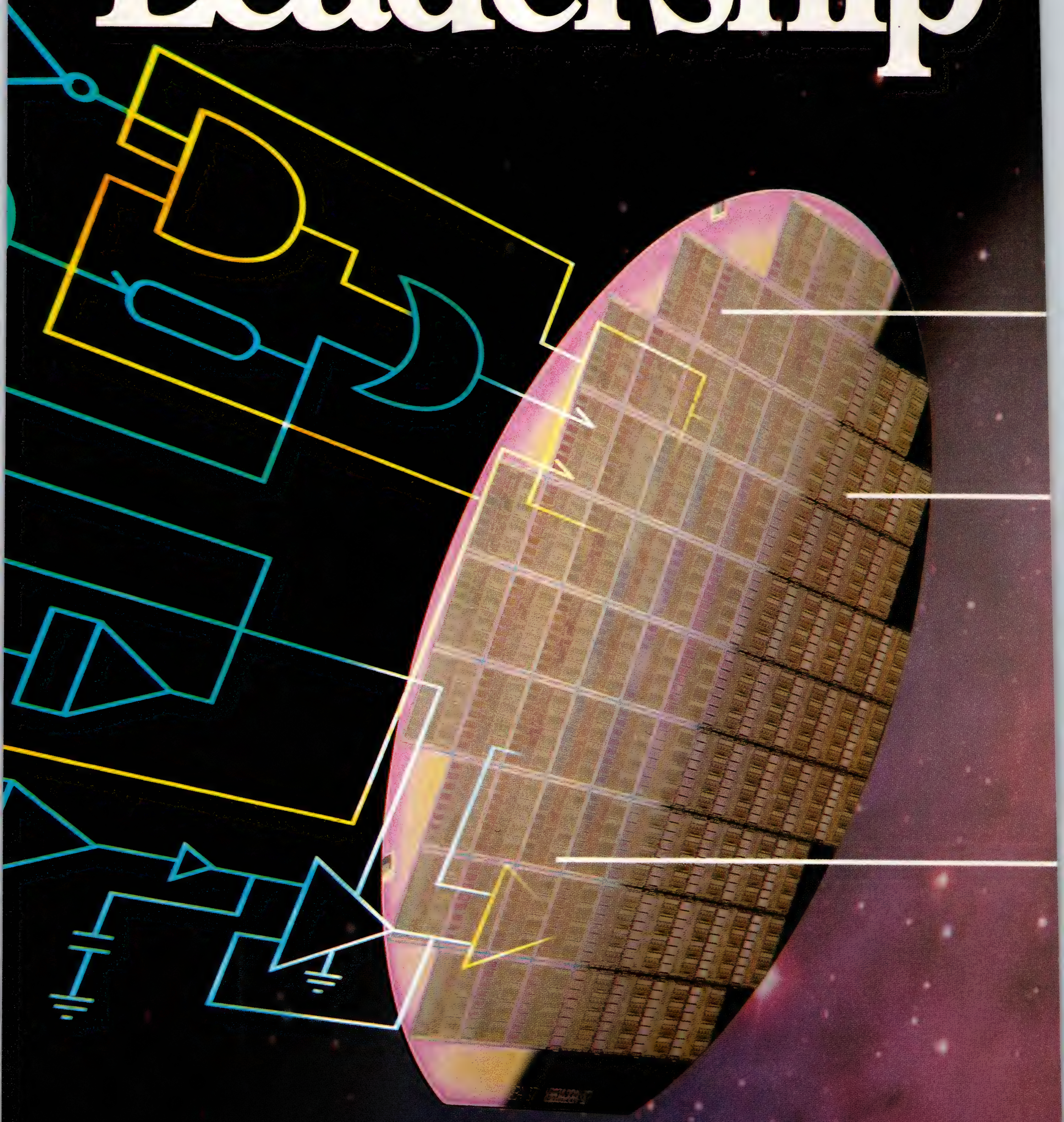
CIRCLE NO 43

Leadership



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Innovation: At Plessey, new ideas, new designs, new applications and new technologies are what we do best and what we do first.

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Leadership means both breadth and depth
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As an ASIC company we supply the world with all manner of ASICs - analog, digital and mixed analog/digital in a variety of advanced state-of-the-art processes. In fine geometry, high density CMOS, bipolar and ECL technologies we provide the highest levels of performance and system integration available today.

As an ASSP (Application Specific Standard Product) company our standard product range offers the highest performance products available in the world today. Capabilities ranging from CMOS devices operating with only 10µA of current to the world's most advanced 1.3 GHz monolithic amplifier.

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Plessey's family of advanced DSP products offer you technology leadership in a variety of advanced image processing applications. For example our DSP 2D Convolver can easily handle 40 million pixels per second and it can be tailored to many specific applications like Medical, Military, or even the motion picture industry. It comes with its own cell libraries - written for DSP- not the typical all-too-general cell libraries others offer. Plessey also leads the way with compression techniques. And it's vital technology because as resolution improves with for example, HDTV, color copiers, color FAX machines or ultra-sonic imaging; disk space can be quickly gobbled up, unless you know how to put the squeeze on your images. Plessey shows you how.

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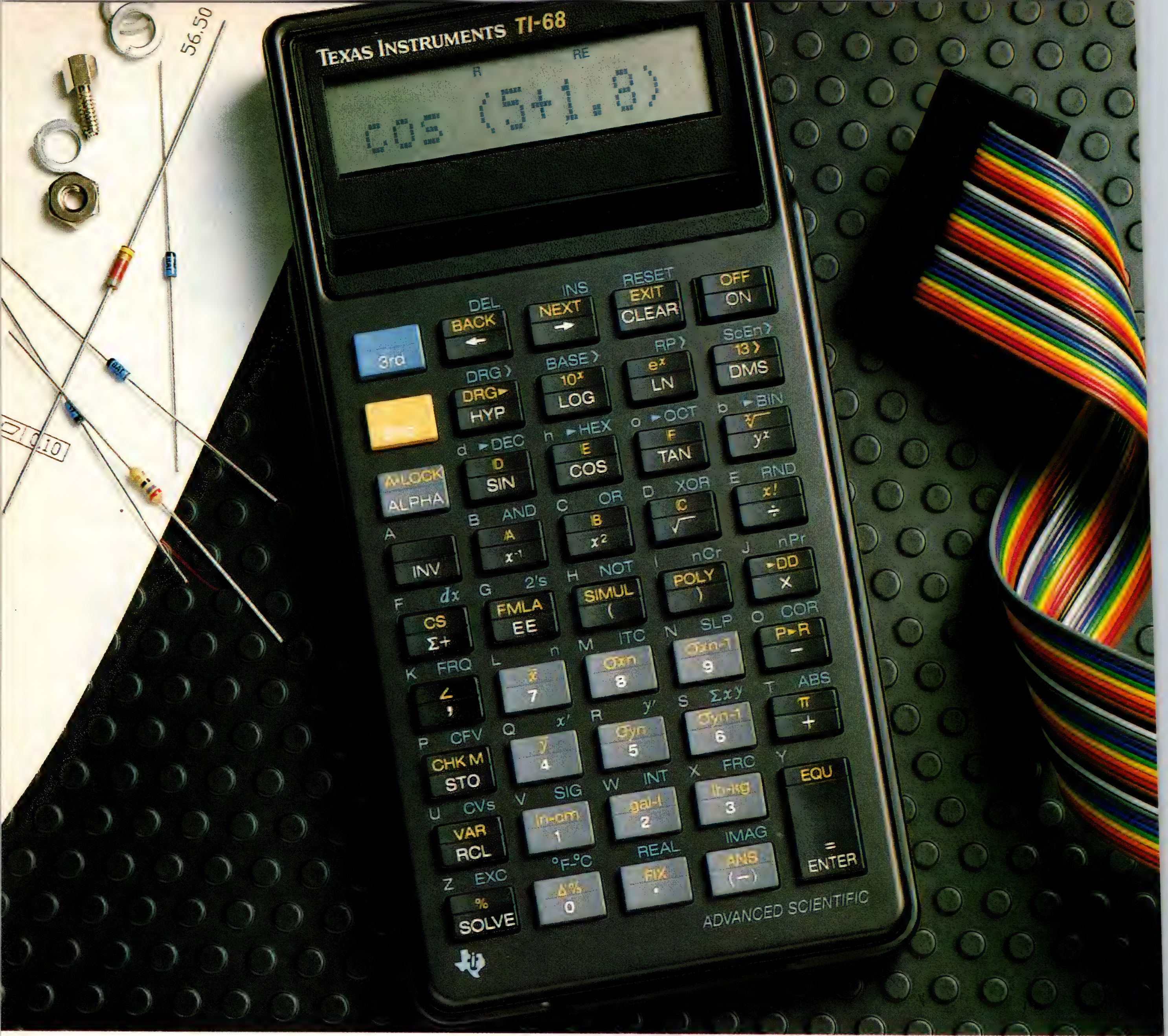

There's a new standard for functionality, ease-of-use and price. The TI-68.

We set some tough goals for ourselves in designing the TI-68. It had to have the powerful functions that technical professionals need. It had to be easy to use. And it had to provide all of this at a substantially lower price than the competition.

We met all of our goals and then some. The TI-68 has 254 useful functions. It solves up to five simultaneous equations with real or complex coefficients. A prompting system guides you through all entries and results. You can handle the complex numbers exactly the way you want, without entering a special mode. The TI-68 evaluates 40 complex number functions and lets you choose polar or rectangular forms for entries and results.

It also lets you easily check your equations with a 12-character alphanumeric display that can scroll through up to 80 characters for long equations. And, the last equation replay feature lets you edit or check the last computation without having to go back and reenter it.

In addition, when you need to solve quadratic, cubic or quartic equations, the TI-68's polynomial root finder will calculate the real and complex roots — automatically.

Working with number bases and conversions are also no problem. Perform arithmetic functions in decimal, hexadecimal, octal or binary. And it does Boolean logic operations, too.

The TI-68 provides up to 440 program steps for as many as 12 user-generated formulas. It even stores up to 36 values in memories with user-defined alphanumeric names.

The TI-68 has what you've been looking for — the right functionality at the right price. See and try it at a nearby retailer, or call 1-806-747-1882 for additional information and to request free product literature.

TEXAS INSTRUMENTS

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CIRCLE NO 45

EDITORIAL

She'll be right, mate

Some years ago when I was visiting Australia, my hosts introduced me to a local saying, "She'll be right, mate." That's the equivalent of today's saying, "Don't worry, be happy." Drivers may also be familiar with the scatological saying affixed to automobile bumpers regarding things that happen. The attitude behind these sayings is a reflection of what's wrong with America today and why we've lost our competitive edge. To be sure, none of us is perfect, but when mistakes and problems occur, we have to be accountable. Beyond that, we have to fix the messes we've gotten into.

Today, we need millions of Americans who are mad as hell and unwilling to take any more indifference from people who get paid to do a job—no matter how meager the pay is. Unfortunately, the "What, me worry?" and "Close enough for government work" attitudes are absolutely endemic in our society. Few of us can survive a day without running into surly clerks who short-change us, part-time workers who give us the wrong laundry, or software-support specialists who know less about a product than we do. Their attitude is, "Don't worry, it will sort itself out somehow—I can't be bothered to fix it now."

The problem reaches to great heights. Watch the evening news or read a newspaper, and you're bound to learn about elected officials and business men and women who really make a mess of things and then tell us not to worry, things will be okay in the end. For example, when a company forecasts a good year but has a miserable one instead and the annual report explains that the poor results were due to market forces beyond management's control, it's time for action. The employees and stockholders should rise up and oust the management. Not because of the company's poor performance, but because of the management's refusal to accept responsibility. In this case, management could act responsibly by eliminating bonuses, taking a pay cut, and enacting other measures necessary when facing a year of poor performance.

As long as we tolerate the irresponsible "She'll be right, mate" attitude, we'll continue losing our competitive edge to people who take responsibility for their actions and willingly correct their mistakes. I'm mad as hell, and I'm not willing to take it any longer. I hope you feel the same way. If you don't, much of what you think you're working for may be already lost.

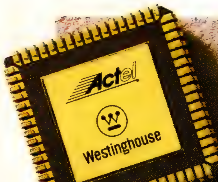
Jon Titus

Jon Titus
Editor

Jesse H Neal
Editorial Achievement Awards
1987, 1981 (2), 1978 (2),
1977, 1976, 1975

American Society of
Business Press Editors Award
1988, 1983, 1981

Logic Int For The



Westinghouse military systems engineers replaced four 22V10 PALs and six MSI devices with a single ACT 1010 part, handling the entire error correction, registration, and interface logic for their high speed, high dynamic range A/D converters. Schematics were captured on a Mentor system, and implemented with the Action Logic System (ALS). The design utilized 224 out of 295 logic modules.

Maxtor engineers use Actel's ACT 1010 chips and the Action Logic System software to quickly create and modify new disk drive electronics. They've produced nine different designs, with 85% to 95% gate utilization. During seven months of intensive work the ALS software has never crashed or lost data, and the system has produced every part as designed.

Actel Field Programmable Gate Arrays.

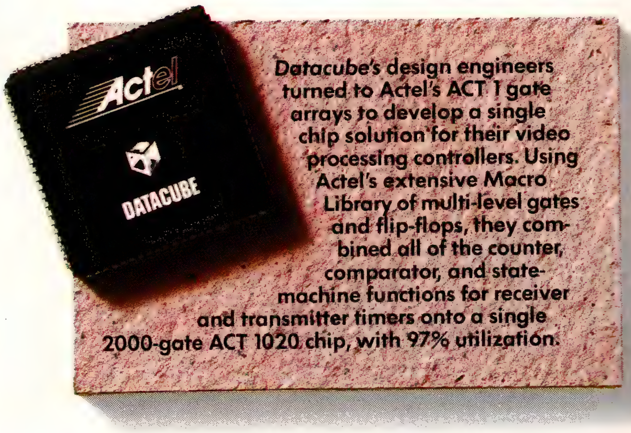
Let's face it. When it comes to programmable ASICs, greed is just good engineering. The best engineers are always hungry for more. More logic. And more different kinds of logic. All on one chip.

More is exactly what you get with Actel's ACT™1 field programmable gate arrays.

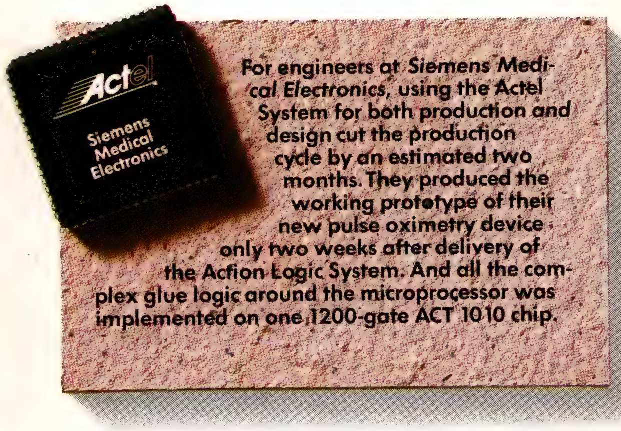
They're a whole new technology designed specifically for logic integration. Not just another brand of EPLD, PAL®, or LCA™ chip. They combine a true channeled gate array architecture with Actel's revolutionary PLICE™ antifuse programming element—resulting in 85% gate utilization. Guaranteed. But you not only get more with Actel, you also get less. Less work, thanks to 100% automatic place and route.

Actel's complete logic solution includes the Action Logic™ System (ALS) software, a programming module, and 1200- or 2000-gate ACT 1 programmable gate arrays.

egration Greedy.



Datacube's design engineers turned to Actel's ACT 1 gate arrays to develop a single chip solution for their video processing controllers. Using Actel's extensive Macro Library of multi-level gates and flip-flops, they combined all of the counter, comparator, and state-machine functions for receiver and transmitter timers onto a single 2000-gate ACT 1020 chip, with 97% utilization.



For engineers at *Siemens Medical Electronics,* using the Actel System for both production and design cut the production cycle by an estimated two months. They produced the working prototype of their new pulse oximetry device only two weeks after delivery of the Action Logic System. And all the complex glue logic around the microprocessor was implemented on one 1200-gate ACT 1010 chip.

Less design entry, with over 150 standard logic functions in the ACT 1 Macro Library. Less design time, with 100% observability of internal logic signals. And less time to market, with finished parts in hours, not weeks or months.

Not to mention much less cost, with no NRE. As in zero.

And the Actel design system is flexible. It works with popular workstations like SUN,™ Apollo™ and 386 PCs. And popular design software like Viewlogic,™ OrCAD,™ Mentor,™ and Valid.™

And it comes in a range of sizes, with 1,200- and 2,000-gate parts today, and 6,000 gates on the way.

So the next time you feel the need for greed, turn to Actel.

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Risk-Free Logic Integration

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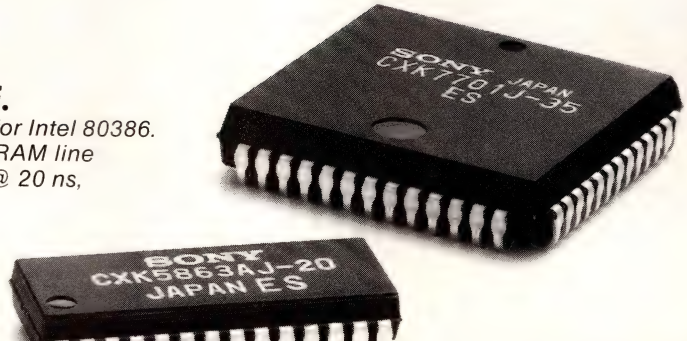
CIRCLE NO 46

SONY TAK
COMMITMENT T

FAST CACHE.
Cache memory for Intel 80386. Also standard SRAM line down to 8K x 8 @ 20 ns, 16K x 4 @ 15 ns.



What you see here is a demonstration of Sony's intense commitment to your each and every SRAM need.

A commitment made even more impressive by the fact Sony's only been engineering and producing SRAMs for just over five years.

And when you consider we're pouring all our resources into SRAM technology—including a new production facility in Nagasaki, Japan—this demonstration merely hints at the Sony SRAM technology yet to come.

Ultra-high speed cache.

Via a unique 0.8-micron process, Sony covers your fast processor cache-memory needs two distinct ways.

First, there's our Model CXK7701J, designed specifically for the Intel 80386.

This application-specific memory (ASM) combines address latch, memory and transceiver within one IC. Ready for user configuration as either an 8k x 16-bit memory or as two 4k x 16-bit memories.

Second, consider our new ultra-high speed SRAM capabilities.

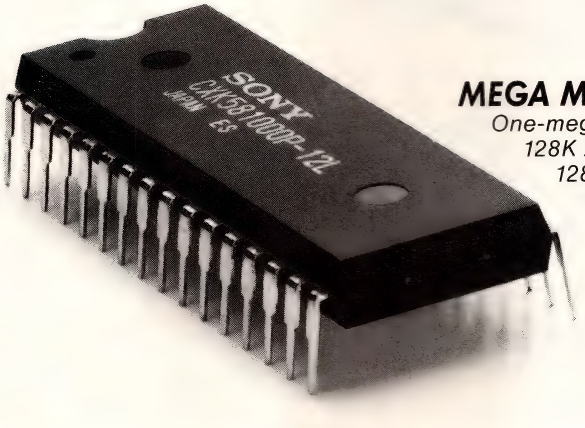
As you scan the chart above, keep in mind even higher speeds will be available soon.

ULTRA-HIGH SPEED CACHE SRAMS

MODEL	CONFIG.	SPEED (ns)	PACKAGE
CXK7701J*	8K x 16	30/35/45/55	PLCC
CXK5863AP	8K x 8	20/25/35	DIP 300 mil
CXK5863AJ	8K x 8	20/25/35	SOJ 300 mil
CXK5466P	16K x 4	15/20	DIP 300 mil
CXK5466J	16K x 4	15/20	SOJ 300 mil
CXK5467P**	16K x 4	15/20	DIP 300 mil
CXK5467J**	16K x 4	15/20	SOJ 300 mil

*For Intel 80386. **O/E

ITS SRAM
THE EXTREMES.



MEGA MEMORY.
One-meg SRAM line includes
128K x 8 @ 100/120/150 ns,
128K x 8 @ 70/85 ns,
128K x 8 @ 35/45/55 ns.

Ultra-high density.

Sony solves your board-space problems with three new 1-Mbit SRAMs.

Each is based on our 0.8-micron CMOS technology. Configured as 128K x 8 bits. And available in 32-pin DIP and surface-mount plastic packages.

And not only do Sony 1-Mbit SRAMs maximize board space, but process speeds as well.

HIGH-DENSITY SRAMS			
MODEL	CONFIG.	SPEED (ns)	PACKAGE
CXK581000P	128K x 8	100/120/150	DIP 600 mil
CXK581000M	128K x 8	100/120/150	SOP 525 mil
CXK581001P	128K x 8	70/85	DIP 600 mil
CXK581001M	128K x 8	70/85	SOP 525 mil
CXK581020SP	128K x 8	35/45/55	DIP 400 mil
CXK581020J	128K x 8	35/45/55	SOJ 400 mil

Nowhere else will you find a greater choice: 100/120/150-ns, 70/85-ns and 35/45/55-ns speed figures.

Sony SRAMS cover the performance spectrum.

Sony offers well over one hundred SRAM solutions, covering the entire performance spectrum.

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We'll go to the extremes to deliver.

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CIRCLE NO 47

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This new ultra-thin sealed lead-acid battery uses a breakthrough construction and manufacturing process that delivers thicknesses as low as 5.7mm. So batteries can be stacked or inserted side-by-side for incredibly slim packaging and complete design freedom.

My-Act also offers a whopping 30% increase in energy density over the F-Act. Not to mention a very competitive price. And every battery is 100% tested to ensure quality and reliability.

Panasonic lead-acid batteries...a class act.

Panasonic offers one of the largest sealed lead-acid battery lines around. And one of the best. Our batteries stand up to tough operating conditions like deep discharge... or overcharge. They're 100% tested. They operate in any position. And they come in a wide range of sizes and power capacities for a multitude of applications.

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CIRCLE NO 48

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Design us in

The IDT6178 has all the features you want to design in: a single-pin block reset for multitasking environments, a totem-pole match output for easy high-speed expansion, 4 K depth to support large caches, industry-standard pinouts, and an on-board comparator to simplify cache controller designs.

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We have the fastest cache tag RAMs available now. And we have packaged the IDT6178 in 22-pin plastic and hermetic DIPs and 24-pin SOJs to meet your various design needs.

We also supply the industry's largest cache tag RAM, the IDT7174, organized 8 K × 8 with all the features of the 4 K × 4 but with the depth to support even the largest caches.

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IDT is offering free samples of our cache tag RAMs now. So don't get left behind—just fill out the coupon and send it in today by FAX or mail to try our cache tags for yourself. Or call our Marketing Hotline at **(800) 544-SRAM** for more information.

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☐ I need IDT's cache tag RAMs today! Please have a salesperson call me.

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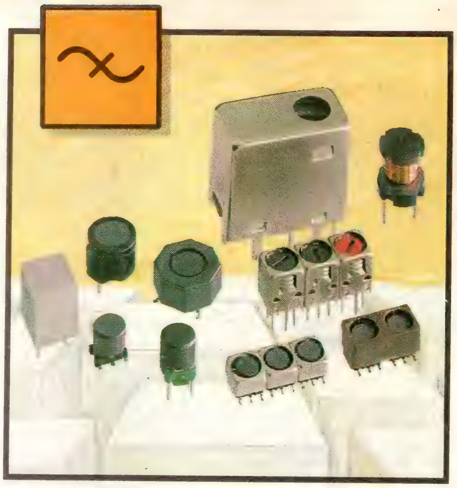

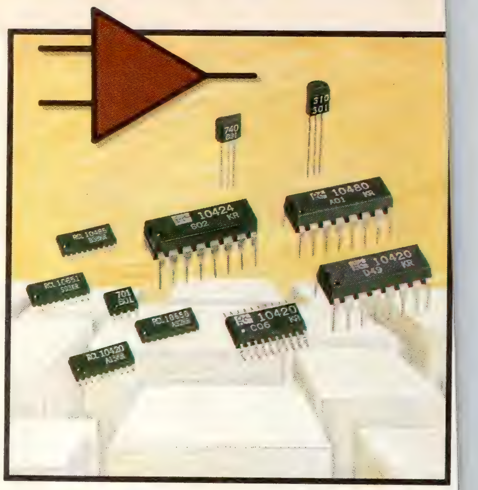

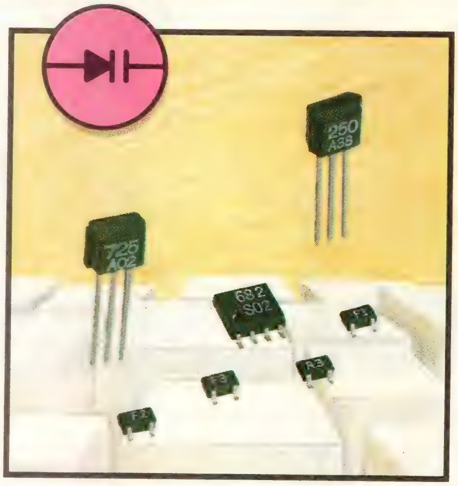

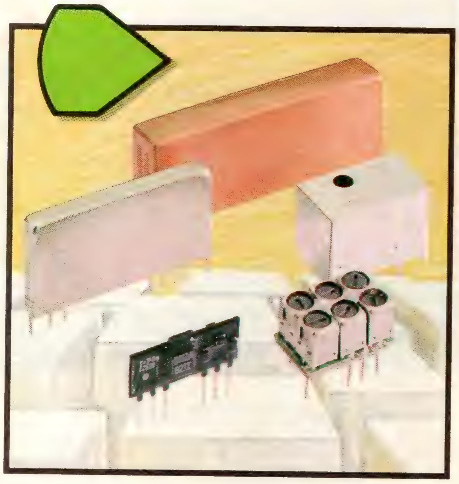

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ASIA

Making it in Taiwan:

Life at a Taipei computer company

Article and photographs by Gary Legg,
Special Projects Editor

中華民國

It's rush hour in Taipei, on a hot and hazy morning. A mass of cars, motorscooters, and motorcycles moves fitfully along Pateh Road, a paved but dusty four-lane street. The buildings on either side are a hodge-podge—some clean and new, others seedy and drab—and almost all are festooned with large, colorful Chinese signs.

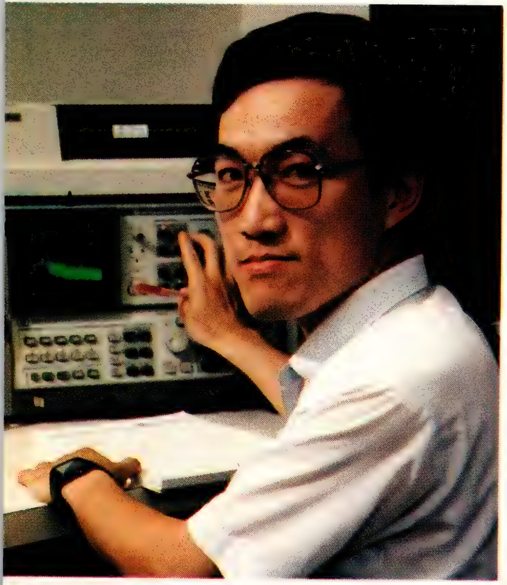
Traffic comes to a crawl; motorscooters thread their way between cars. It speeds up again; cars zip by cyclists with only inches to spare. A dozen or so scooters move in unison like a school of fish, seeking protection in numbers from the predator automobiles. Some of their riders wear surgical masks or bandanas to filter the ever-present haze of exhaust.

One of the cyclists, neatly dressed in slacks and a white, open-neck shirt, pulls out of traffic in front of a modern, seven-story building. He parks his Vespa 125 on the sidewalk in a row of other two-wheelers, enters the building's air-conditioned coolness, and takes the elevator to the second floor. Waving to the receptionist, he walks through the small lobby and into the R&D lab of DTK Computer. For electronics engineer David Wang, 29, it's the start of a new workday.

Taipei's ubiquitous motorscooters, here on Pateh Road (the location of DTK Computer's R&D lab), move thousands of commuters every day.

Like Wang's other workdays as supervisor of DTK's quality-assurance department, this one is eight hours long officially and ten hours or so unofficially. Saturday is half a workday—four hours. Wang earns about $20,000 (U.S.) a year for his efforts, plus three to five months' salary in annual bonuses. Though his hours are long, he doesn't have to punch a time clock, as he would at many Taiwan companies, and DTK's flex-time policy allows him to begin work anytime between 7:30 and 9:30.

This article is the first in a series that will examine the electronics-engineering profession in Asia.



David Wang, supervisor of the quality-assurance department, conducts a noise-emission radiation test.

It's just after eight now, and as Wang stands and looks across the open lab, he sees some colleagues already at work. A few desks away, hardware designer Benjamin Hsieh stares intently at his workstation screen, oblivious to everyone around him. Near the back of the lab, R&D assistant manager Simon Ho casually drapes an arm across an engineer's shoulders, offering encouragement and camaraderie. An engineer hooks up an in-circuit emulator on a workbench. Someone walks by with a PC chassis.

Personal space for engineers is never plentiful in Taiwan, and recent rapid growth has made room at DTK even scarcer than usual. Employees at the company's Taipei R&D center increased from 45 to 72 in the last year, and until the lab moves to a new location later this year, it will remain cramped. The crowded lab contains desks as well as workbenches. The small, two-by-four-foot desks are arranged loosely in rows. An occasional bookcase provides storage; books and papers are stacked all around on small tables.

Still, despite the growth that took it from start-up status to a 1000-employee company in eight years, DTK remains relatively streamlined. Only one layer of management lies between quality-assurance supervisor Wang and DTK president Duke Liao. Wang typically gets purchase-order approval for new test equipment in two weeks; at 4000-person Acer, the leading Taiwan computer company where he worked until earlier this year, two months was the norm.

Streamlined operation may have helped DTK achieve its position as a leading supplier of PC mother boards, but the company's plans are more ambitious now. To sustain its growth, DTK is emphasizing complete systems, from 10-MHz, 8088-based models to 33-MHz, 80386-based systems, as well as a 10-MHz, PS/2 Model 50 clone. The company also has a laptop computer in the works, and it recently started developing an engineering workstation based on the Sun Microsystems SPARC chip set.

Keeping up with all the different computer architectures is the re-

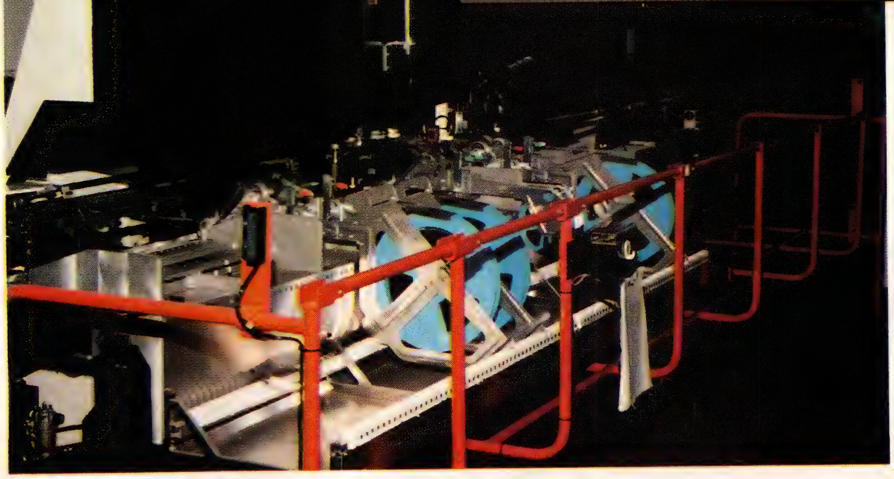
Engineering salaries in Taiwan: $8600 a year for a new grad to $30,000 or more for an assistant manager of R&D.

sponsibility of the 12-person architecture group in the Systems Development Department, headed by Norman Tsai. Most members of the group studied architectures as part of their college electrical-engineering curricula. They're assisted in their research efforts, as are many Taiwan high-tech companies, by information from the Institute for Information Industry (III), an agency of the Taiwan government.

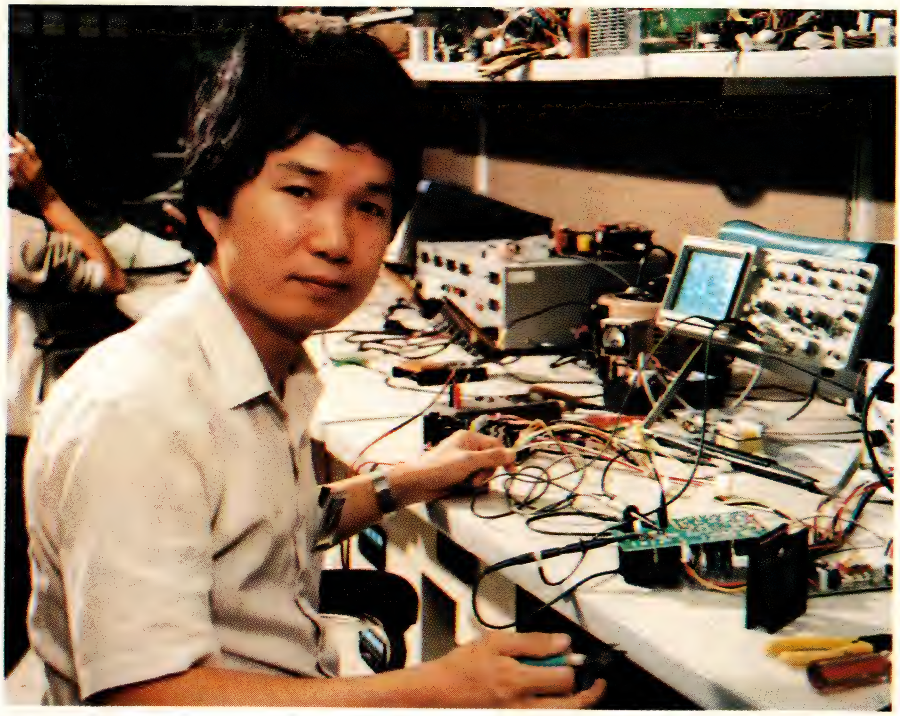
Like most PC-clone companies, DTK uses clone chip sets from companies such as Chips & Technologies and VLSI Technology. Unlike many other clone companies, it also develops its own chip sets. In fact, the company's R&D department is divided into two divisions: systems and ASICs. The ASIC division, under R&D chief Dr. Chen Kunnan, employs 20 engineers. Most of these engineers learned ASIC design through in-house training and experience. Some also have attended ASIC vendors' seminars. Another important source of information to the group is the Electronics Research Service Organization (ERSO), a government agency that's similar in function to the III, except that it concentrates on VLSI technology.

To support its chip-design effort, DTK uses a variety of computer-aided-engineering tools. In its inventory is an ECAD Dracula design-rule checker, a Daisy Logician simulator, a Micro VAX II workstation, EGA workstations, and an ASIX II VLSI tester. The ASIC group currently has about four engineers sharing each workstation, but the number of workstations will increase now that DTK is manufacturing its own 80386-based computer.

Although designing its own PC chip sets is costly in terms of engineering time, developing them in house provides two advantages, says marketing planning manager Sam Tsai. One is that, after chip development, DTK can choose from its own and outside vendors' sets according to cost effectiveness and performance characteristics. The other advantage—less tangible—is the extra knowledge and insight gained by DTK engineers; as a result of chip-development efforts, says Tsai, "Our guys have schemat-



DTK's R&D lab is in a modern building that also houses a small hospital and other businesses. Prototype assembly takes place in a building across the street that looks shabby but contains state-of-the-art, surface-mount manufacturing equipment. Later this year, DTK will move to a modern facility now under construction.



R R Lee, an assistant manager of research and development, directs the design of switching power supplies.

ics in their heads." Chip-development costs, he insists, are often offset by the short time to market for new products that such insight affords.

DTK also defies conventional strategy by offering its own BIOS software. Software manager David Chang, 35, says DTK BIOS development began several years ago, when long-term availability and second sourcing of BIOS routines from outside vendors were uncertain. Now such software is readily available, but the company continues its own development for the same reason it develops its own chip sets—to gain technical insight and to have a cost-effective alternative. DTK has proprietary MS-DOS BIOS software for 8088-, 80286-, and 80386-based systems, and work is proceeding on a BIOS for OS/2. The company does provide other vendors' software when customers request it, however.

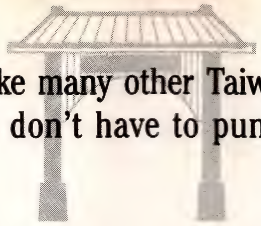
Of all the work-related problems at DTK, the shortage of physical space is perhaps the greatest. The problem is almost critical in the quality-assurance department, which grew from six to 17 people in just the first half of this year.

Profile: Taiwan

Although references to the "country" of Taiwan are common, many of Taiwan's 20 million residents would dispute that designation. To them, their 250-mile-long island is simply a province of China—and the seat of China's lawful government, in exile since the Communist takeover in 1949. Officially, the designation is Taiwan, Republic of China. The capital city is Taipei.

Even though the Taiwan government lost United Nations recognition in 1971, Taiwan is nevertheless a de facto nation to much of the world, albeit sometimes without official diplomatic ties. Taiwan's volume of trade is the 13th largest in the world; after Japan, it has the world's second largest foreign-exchange reserves.

Taiwan's electronics industry accounts for some $16 billion a year in revenues, $13 billion from exports. The Taiwan government encourages and subsidizes high-tech development through agencies such as the Institute for Information Industry (III) and the Electronics Research Service Organization (ERSO). The government also sponsors projects such as the Hsinchu Science-Based Industrial Park, located about 50 miles south of Taipei.



At DTK, unlike many other Taiwan companies, engineers don't have to punch a clock.

Supervisor Wang needs space not only for his people, but also for an open-site test area to meet American FCC requirements. He expects his problems to be solved later this year, when the company moves to a new facility that has more office space and a rooftop test area. In the meantime, he dismisses the space problem and concentrates on training his staff to conduct tests at the increasingly high clock rates of DTK's expanding computer line.

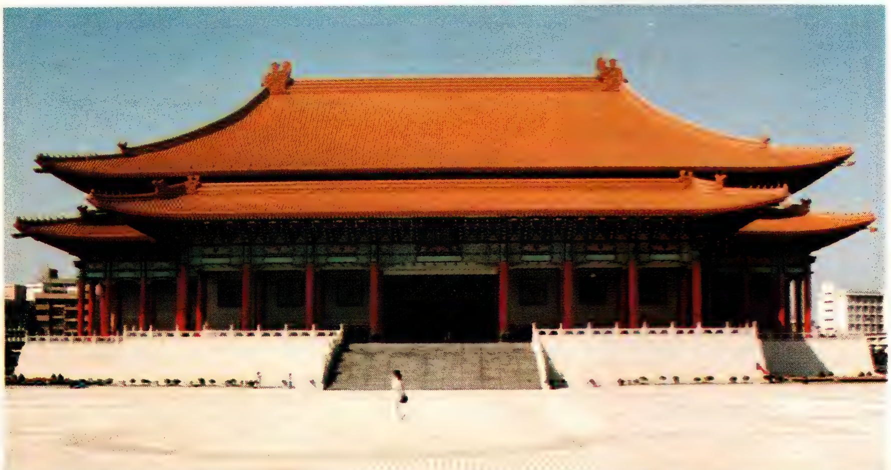
On-the-job training of all types is a prominent part of life at DTK. Each technical department selects a weekly topic for study—switching-power-supply safety standards, for example, or memory-design techniques—and then presents a seminar on its findings. Selected DTK engineers also attend in-house management classes.

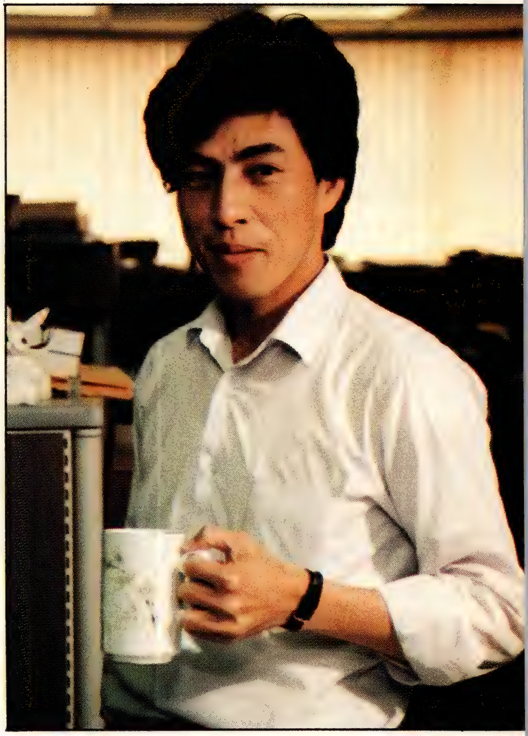
Wang, like many engineers, views management responsibilities with ambivalence. Asked if he enjoys being a manager, he responds with a deep sigh and begins a general discourse on management pros and cons. Then, suddenly realizing that he's dodging the question, he decides to face it head-on. "You ask if I like management?" he laughs. "I hate it."

As a manager, Wang explains, he must be diplomatic and "treat everyone as my friend," when what he's really concerned with is his technical work. Nevertheless, he knows management is his future, especially if he eventually starts his own company, as he sometimes daydreams. Wang's personal goal is for management to be his major work within eight years, by the time he turns 37.

The chief attraction of management for Wang isn't money, but the greater authority and broader view. A realist, however, he knows he will pay a price in increasing remoteness. He recites a Chinese saying and then translates it: "The great men are always lonely." Informed of the English-language equivalent, "It's lonely at the top," his eyes glint in recognition and a pensive smile appears. "Yes," he nods, "yes."

Wang's ambivalence notwithstanding, management positions generally are coveted in Taiwan, possibly because of the gap between management and nonmanagement salaries. A beginning engineer at DTK, for example, earns about $8600 (U.S.) a year, in sharp contrast with Wang's $20,000 plus substantial bonuses. A notch up from Wang, assistant R&D manager R R Lee draws a $26,000 salary, plus bonuses, for directing power-supply development. For leading software efforts, fellow assistant manager David Chang earns $31,000 and bonuses.

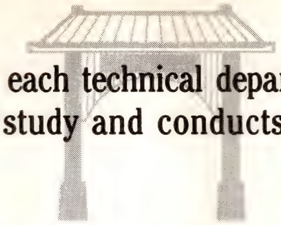




R&D assistant manager Simon Ho, whose responsibilities include all peripheral development, takes time out for tea.

For Wang and his colleagues, salaries such as these help provide a satisfying lifestyle in Taiwan. Wang was lucky, however, in that he was able to buy an apartment in Taipei two years ago, before housing prices took a dramatic rise. The value of his apartment, which occupies the single floor of a multistory building, has soared since then—from 2.5 to 11 million New Taiwan dollars. The current value in US currency is approximately $440,000.

Comfortably at home in Taipei, Wang enjoys the city's 24-hour-a-day hustle and bustle. On a three-week business trip to the U.S. last



Every week, each technical department selects a topic of study and conducts a seminar.

Hardware designer Benjamin Hsieh designs digital circuits in DTK's R&D lab. At the far end of the room is the mechanical-design section; the peripheral-design area is in between.

year, he found American cities, with the exception of New York and Las Vegas, to be lonely and sterile. "What do people do at night?" he asks.

It's only for a change of pace that Wang leaves the city. After church on Sunday (he's one of the few Christians in Taiwan), he and his wife and their two young sons may climb into their '89 Renault 21 and head for the suburbs or the nearby mountains. The mountains are popular with many Taipei residents because they're easily accessible and offer relief from heat and pollution.

Unlike Wang, power-supply guru Lee and software leader Chang consider city life something to be tolerated rather than enjoyed. Both live in a part of Taipei that's only a 20-minute drive from DTK, but still near the mountains. Lee, 36, says that finding a place to live away from Taipei's mad rush was his first consideration when deciding to join DTK.

Lee frequently hikes in the mountains for the exercise and fresh air. He likes to unwind on Sundays with his two children and play mahjong with his wife and another couple. Chang, who grew up in a quiet coastal town, keeps in touch with his seaside roots by surf fishing. Like Lee and Wang, he has two children.

Part of the satisfaction that Wang, Chang, and Lee feel in their lives may well be due to the high status of engineers in Taiwan, where electronics is an important and glamorous part of the economic picture. Part of that satisfaction may also be the progressive attitudes of DTK management toward its employees. Engineers at DTK frequently use terms such as "open" and "breathing space" and "nice environment" to describe their work life.

But the most important contribution to DTK engineers' satisfaction may simply be freedom to face challenges. "It's a very open company," Chang says. "If you have an interest and capability in a certain area, you're free to run with it." EDN

Acknowledgment

The author is grateful to Tom Bayens of DTK Computer's California office for arranging interviews, serving as interpreter, and providing background information.

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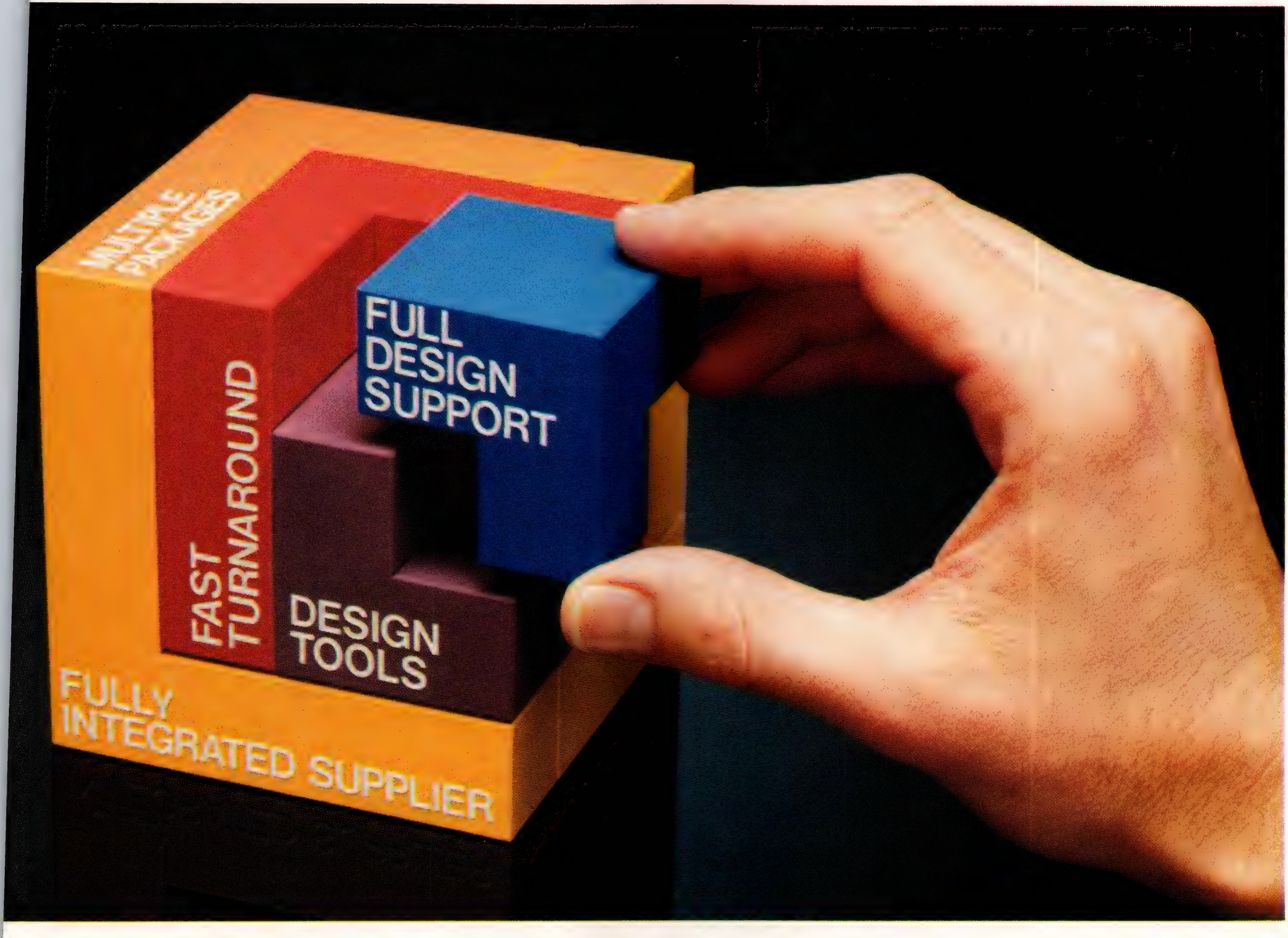

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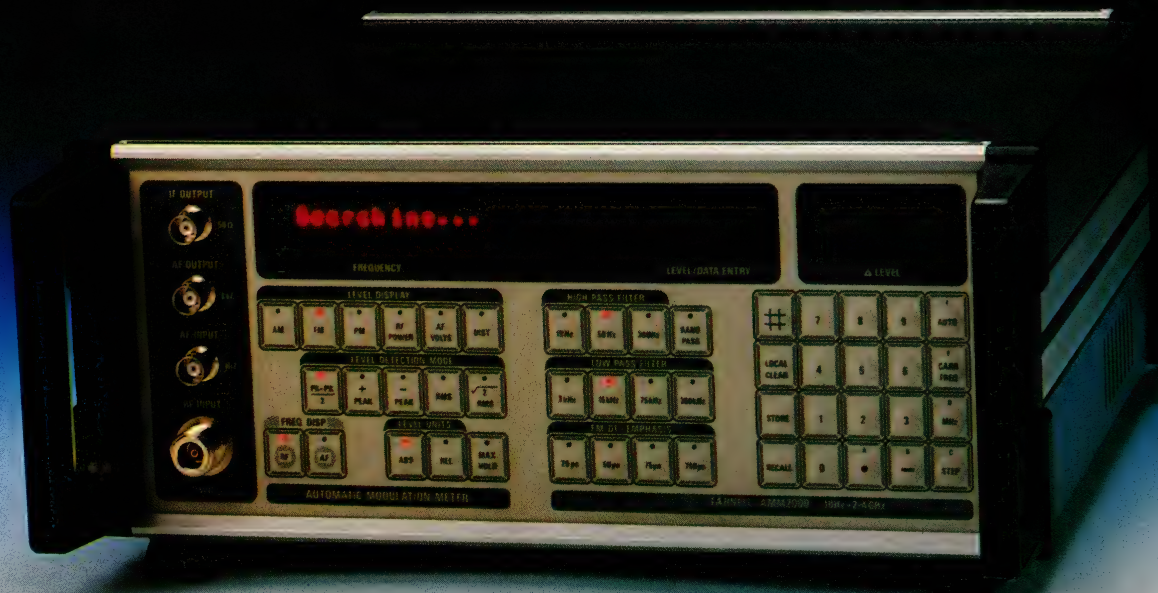

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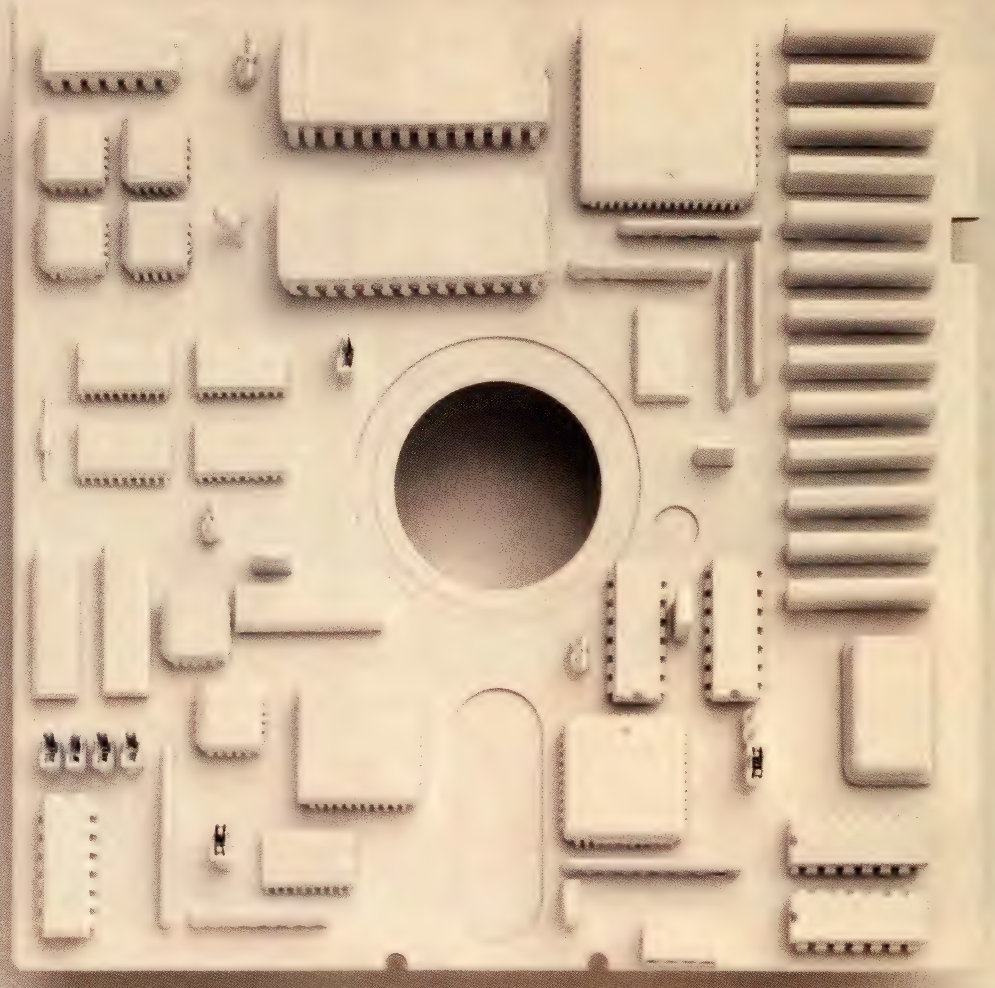

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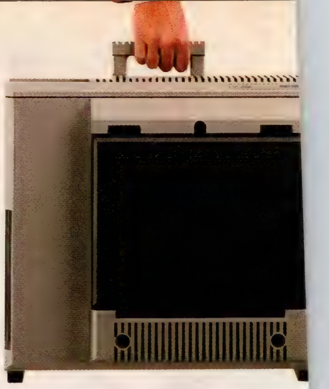

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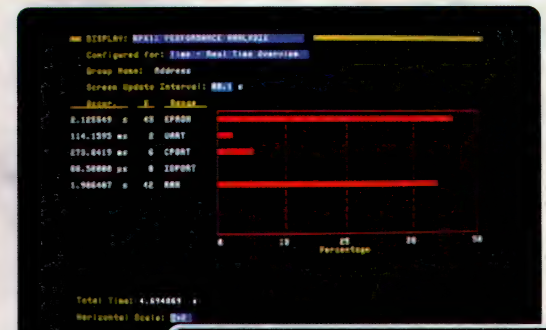
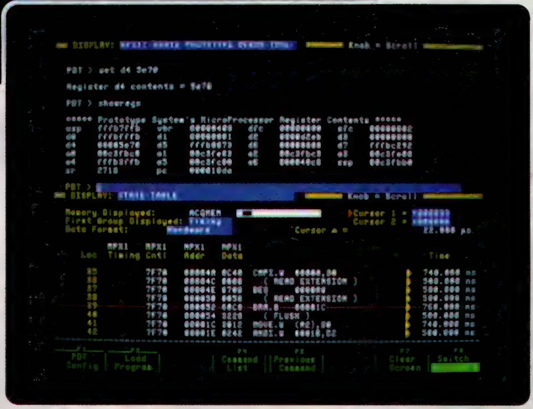
Now digital designers and integrators can start with all the speed, channels and memory depth they need— without tradeoffs. They can mix-and-match tools for their specific needs, including 8, 16 and 32-bit microprocessor debug modules brimming with features never before possible in a logic analyzer. They can add other modules, such as for high-speed timing and waveform analysis, later.

The new dimension of hardware/software integration.

- Microprocessor control
- Real-time performance analysis
- 200 MHz timing
- 8K deep state analysis
- Multiple microprocessor support





You can view 200 MHz timing and 8K of state data per channel, all time-correlated and integrated on the same display.

Observe data from multiple microprocessors or timebases simultaneously. Set up

(Above, left) Real-time performance analysis as displayed on the Prism color monitor. (Left) The Prototype Debug Tool provides easy access to microprocessor control and debug functions, including the ability to set hardware and software breakpoints, and to patch registers and memory.

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The Prism 3002P configuration features a slide-away keyboard and a 640x400 flat panel display that folds against the mainframe when not in use.

state and timing sections to cross-trigger, synchronize and arm each other, so you know exactly when and in what time relationship events occur.

Push beyond microprocessor observation into emulator-like microprocessor *control*.

With its unprecedented Prototype Debug Tool, Prism is the first logic analyzer to let you set breakpoints, patch registers and memory, restart the system, and more—without an emulator's intrusiveness (or the long wait for new emulator availability).

Use real-time performance analysis to get a true, non-statistical view of system performance.

Designers of embedded control systems will especially benefit from histograms of uncompromising accuracy.

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Oil painting by
Francis Livingston
San Anselmo, California

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UNIVERSAL-INPUT POWER SUPPLIES

Units suit power needs around the world

Today's universal-input supplies eliminate, among other things, the possibility of mistakenly supplying 220V ac to a device strapped for 110V ac operation.

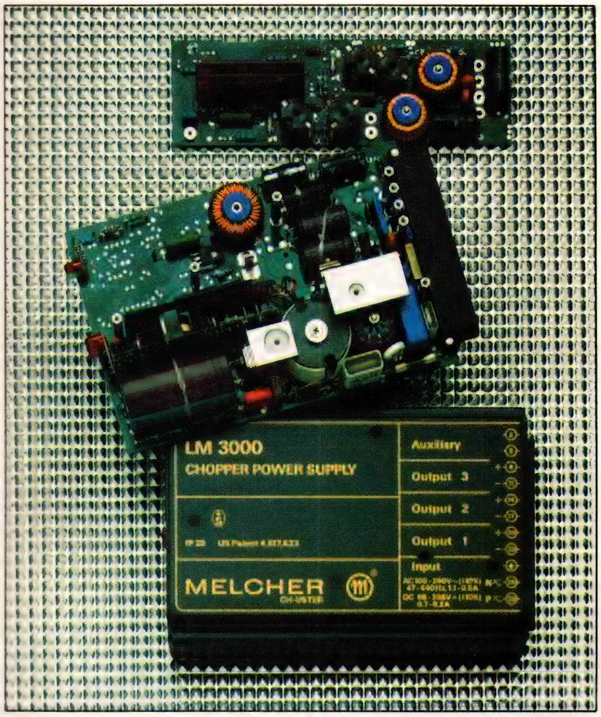
Tom Ormond,
Senior Editor

To compete in worldwide markets, manufacturers of ac/dc power supplies must ensure that their products accommodate a wide range of inputs. Traditionally, power-supply vendors have used either a moveable jumper or a slide switch to change a supply's input capability from 110 to 220V ac. These very basic approaches, though commonly used, do have drawbacks. First, vendors have to know—and never lose sight of—the ultimate end market (domestic or foreign) for the power supply. Second, there's always the possibility that a supply strapped for 110V ac operation will have a 220V ac line voltage mistakenly applied to its input. Make this oversight and you can easily destroy the supply.

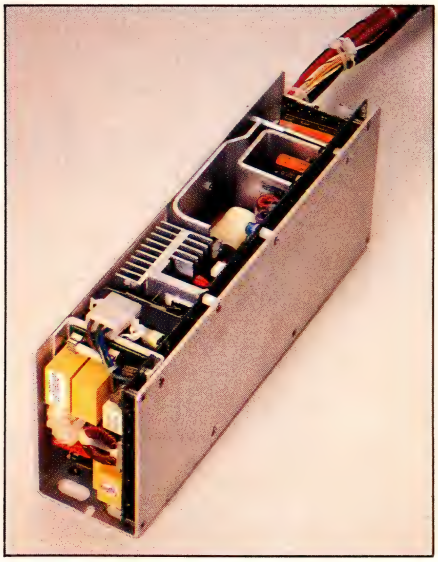
To overcome these problems, a number of power-supply vendors now offer products that can operate anywhere in the world—without the risk of user mistakes at the input stage. These supplies accept inputs ranging from 85 to 265V ac, so users don't have to change jumpers or switch positions.

Most manufacturers employ one of two techniques to develop this universal-input capability. The first approach **(Fig 1a)** typically employs a single-transistor, current-mode flyback design, which allows the supply to operate over the full 85 to 265V ac input range. Yet it also creates a reliability problem in that as you increase voltage, the switching transistor must handle twice the collector current at the low range; the output rectifiers then handle twice the reverse-voltage levels. As a rule, most vendors only use this approach in lower-power supplies (70W and under), where the use of flyback designs reduces the reverse-rectifier voltage levels to normal values.

The second design scheme **(Fig 1b)** employs circuitry that senses the line voltage being applied to the power supply. The circuitry—consisting of a voltage sensor, a low-frequency oscillator, and an electronic switch (triac)—monitors the ac peak input. If the peak is



Featuring a 79% efficiency rating, *Melcher's LM 3000 supplies operate over a −25 to +71°C range and provide three isolated outputs and a 45W output capability.*



Designed for workstation applications, *the PS-575 supply from Brown Applied Technology features five regulated outputs and a 575W output-power capability.*

below 190V, the oscillator enables and provides gating pulses to the triac. When the triac fires, the supply is configured as a voltage doubler for operations having 110V ac inputs.

When the peak value of the input line voltage exceeds 190V, the voltage sensor shuts the oscillator down and stops the triac from firing. The supply then returns to its full-wave-bridge configuration to accept 220V ac inputs. You cannot use this scheme to operate over the entire wide-input range—it's an automatic either/or situation. Nevertheless, the design is such that your supply suffers from virtually no power limitations.

Regardless of the technique employed to develop the wide-input capability, the resulting power supplies **(Table 1)** are quite versatile. As the **table** illustrates, wide-input supplies can meet a range of applications.

When shopping for a wide-input supply, you'll notice two things. First, you have much to choose from; second, you don't have to buy more supply than you need to take advantage of wide-input capability. Melcher and Total Power, for example, offer single-output models in their lines of wide-input devices. Kepco offers an extensive line of single-output supplies with power ratings that span a 15 to 50W range. Also, though many of the wide-input supplies are low-power units, you can find several high-power supplies. Computer Products offers

TABLE 1—REPRESENTATIVE POWER-SUPPLY MANUFACTURERS

VENDOR	PRODUCT	OUTPUTS (VOLTS)	TOTAL POWER (WATTS)	REGULATION (%)		EFFICIENCY (%)	RIPPLE/ NOISE (mV p-p)	OPERATING RANGE (°C)
				LINE	LOAD			
BROWN APPLIED TECHNOLOGY INC	PS-575	5, 12, −12, 18, −5.2	575	±5.0	±5.0	NOT SPECIFIED	50	0 TO 50
COMPUTER PRODUCTS	NFS350	5, 12, −12, 4.5 TO 16.5, 15 TO 30	350	±0.1	±1.0	70	50,120	0 TO 50
CONDOR INC	PAC SERIES	5, 12, −5, −12, 15, −15, 24	85 TO 185	NOT SPECIFIED	0.5 TO 4.0	70±5	1.5%	0 TO 50
CONVERTER CONCEPTS INC	VL 50	5.1, 12, −12, 15, −15	50	0.1	1 TO 4.0	70	2.0%	0 TO 50
ELPAC POWER SYSTEMS	WRI 4212	12	42	±0.2	±4	NOT SPECIFIED	±1%	0 TO 40
KEPCO INC	FAW SERIES	5, 12, 15, 24	15, 25, 50	1.0	1.0	70 TO 76	10 TO 20/ 120 TO 310	0 TO 71
MELCHER INC	LM SERIES	5.1, 12, 15, 24	40, 50	NOT SPECIFIED	NOT SPECIFIED	76 TO 83	NOT SPECIFIED	−25 TO +71
MODULAR DEVICES INC	PS2127	5, 12, −12, −5.2, 24	275	0.2	NOT SPECIFIED	75	NOT SPECIFIED	0 TO 50
POWER GENERAL	FLU2-40	5, 12, 15, 24, 28	40	0.2, 0.5	1.0, 3.0	65	1%	0 TO 70
	FLU3-40	5, 12, −12, −5, 15, −15, 24	40	0.2, 0.5	1.0, 3.0	65	1%	0 TO 70
PREFERRED ELECTRONICS INC	LOP-40-103	5, 12, −12	35	NOT SPECIFIED	1.0, 5.0	75	20, 50/150, 290	0 TO 50
	CDS-175-104	5, 5, −5, 12	175	NOT SPECIFIED	2.0	65	50, 100/200, 300	5 TO 40
TOKO AMERICA INC	MW-50	5, 12, 15	50	NOT SPECIFIED	NOT SPECIFIED	65	NOT SPECIFIED	0 TO 60
	MW-100	5, 12, 15, 24	100	NOT SPECIFIED	NOT SPECIFIED	65	NOT SPECIFIED	0 TO 60
TOTAL POWER INTERNATIONAL INC	TPSU 10	5, 12	10	±0.2	2, 5	70	1%	0 TO 50
	TPSU 40	5, 12, 15	40	±0.2	2, 5	70	1%	0 TO 50

a quad-output 350W unit; Brown Applied Technology features a 5-output supply with 575W of output power.

For the most part, today's wide-input, multiple-output supplies provide the 5, 12, and 15V levels that have become de facto standards. However, some supplies also offer output levels that are designed to accommodate oddball applications. For example, the fourth output on Computer Product's NFS350 supply is a floating output that is user-adjustable over a 4.5 to 30V range. The output can be referenced as either positive or negative. As such, this output can be quite useful for driving loads such as valves, SCRs, and disk drives.

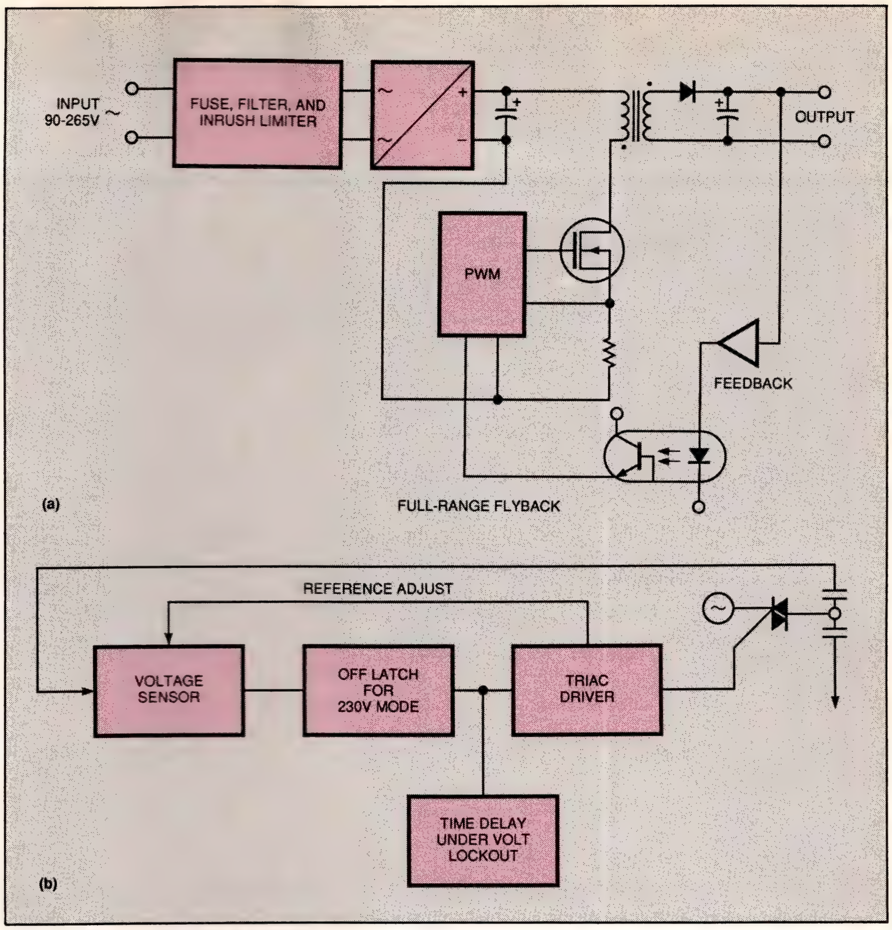


***Fig 1—To accommodate low-power demands,** supply vendors typically employ a single-transistor, current-mode flyback design **(a)** to provide an automatic 85 to 265V ac input capability. For power levels above approximately 70W, vendors generally employ a triac-based circuit **(b)** that automatically switches between the high and low input ranges.*

Wide-input supplies exact no tradeoffs when it comes to output protection. All manufacturers offer overvoltage protection on the main output, and Melcher provides overvoltage protection on all outputs of its multiple-output supplies. As for output current, all manufacturers provide overload protection; most also offer supplies that feature automatic-reset short-circuit protection. Computer Products offers thermal protection as a standard feature as well.

MTBF (HOURS)	FREQUENCY (kHz)	PRICE
60,000	67	$400
45,000	NOT SPECIFIED	$319 (100)
NOT SPECIFIED	NOT SPECIFIED	$175 TO $240
NOT SPECIFIED	100	$34
NOT SPECIFIED	NOT SPECIFIED	$74 (100)
NOT SPECIFIED	120 TO 130	$55 TO $110
NOT SPECIFIED	NOT SPECIFIED	FROM $315 (100)
NOT SPECIFIED	NOT SPECIFIED	$295 (100)
205,000	40	$71
205,000	40	$71
100,000	NOT SPECIFIED	$52 (1000)
30,000	NOT SPECIFIED	$140(1000)
NOT SPECIFIED	80 TO 200	$98
NOT SPECIFIED	80 TO 200	$178
NOT SPECIFIED	NOT SPECIFIED	$39.80 (100)
NOT SPECIFIED	NOT SPECIFIED	$67

You also have nothing to worry about when it comes to agency approvals. Every supply listed in the **table** meets FCC emission standards. Additionally, most of the supplies listed meet VDE, UL, IEC, and CSA safety requirements.

Given this overview of supply capability, it's obvious that there are no wide-input versus performance tradeoffs to consider. The bottom line is cost.

Compared to using a moveable jumper or a slide switch, both of the design approaches used to handle the wide-input-voltage capability for ac/dc supplies do exact a slight cost premium, in that they are more expensive to implement in the devices. However, when you consider that you will reduce installation labor costs and eliminate the possibility of power-supply destruction due to improper input connections, it's clear that you can readily offset the increased up-front investment. You will also reduce your part-maintenance cost, narrow your inventory, and virtually eliminate field-replacement expenses. **EDN**

Text continued on pg 78

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For more information . . .

For more information on the universal-input power supplies discussed in this article, circle the appropriate numbers on the Information Retrieval Service card or use EDN's Express Request service. When you contact any of the following manufacturers directly, please let them know you saw their products in EDN.

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Kepco Inc
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Flushing, NY 11352
(718) 461-7000
FAX 718-767-1102
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Melcher Inc
200 Butterfield Dr
Ashland, MA 01721
(508) 881-4715
FAX 508-879-8669
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Modular Devices Inc
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(213) 542-8561
FAX 213-371-6331
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Power General
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Canton, MA 02021
(617) 828-6216
FAX 617-828-3215
Circle No 708

Preferred Electronics Inc
Box 248
Westfield, MA 01086
(413) 568-2301
FAX 413-562-7275
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Toko America Inc
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Mt Prospect, IL 60056
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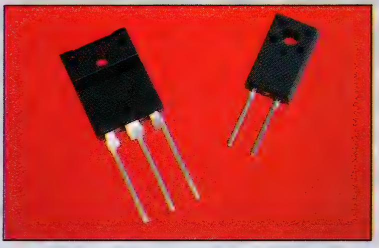
For more information, contact General Instrument Corp., Power Semiconductor Division, 600 West John St., Hicksville, NY 11802. Phone (516) 933-3333.



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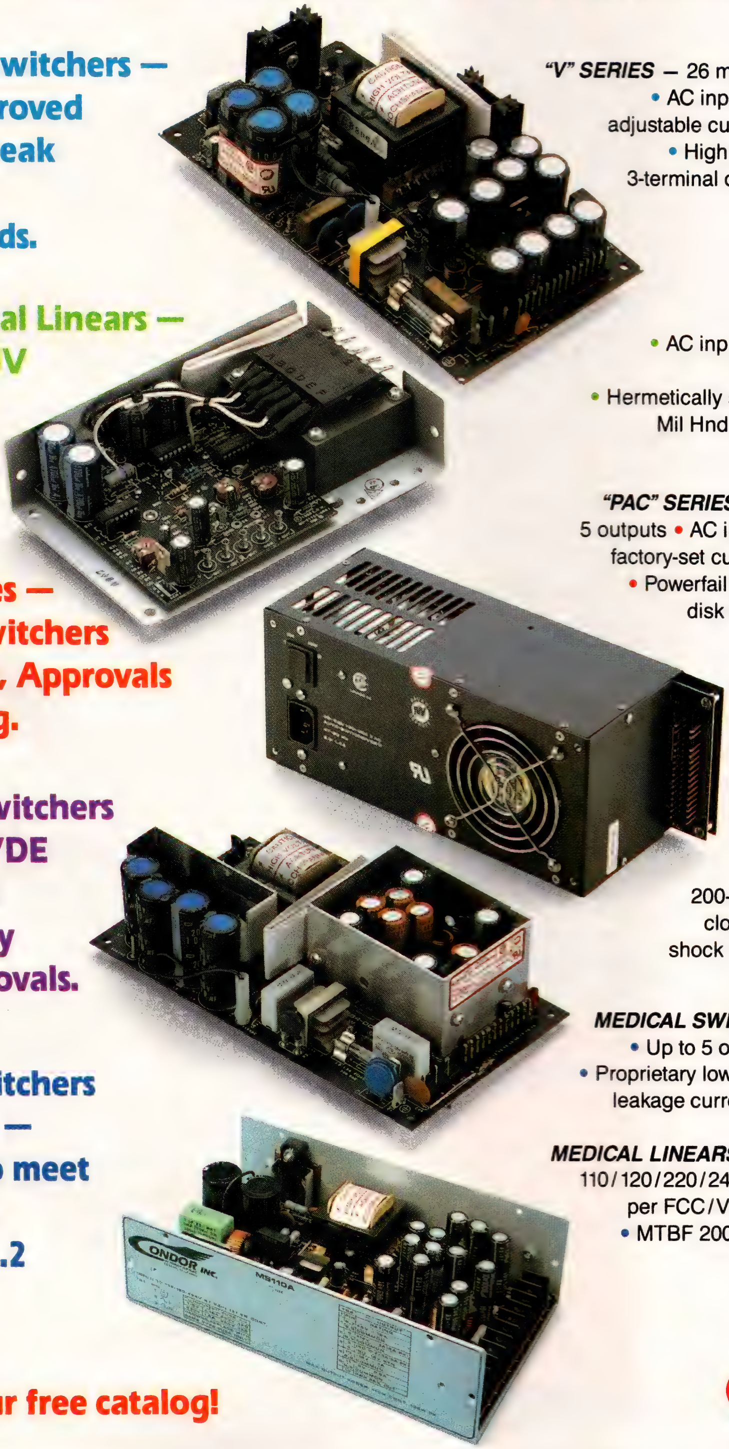

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5V/180A	12V/15A	12V/15A	5V/5A
5V/180A	15V/12A	15V/12A	5V/5A
800w			
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5V/120A	15V/12A	15V/12A	
5V/120A	12V/12A	12V/12A	5V/5A
5V/120A	15V/12A	15V/12A	5V/5A

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CIRCLE NO 59

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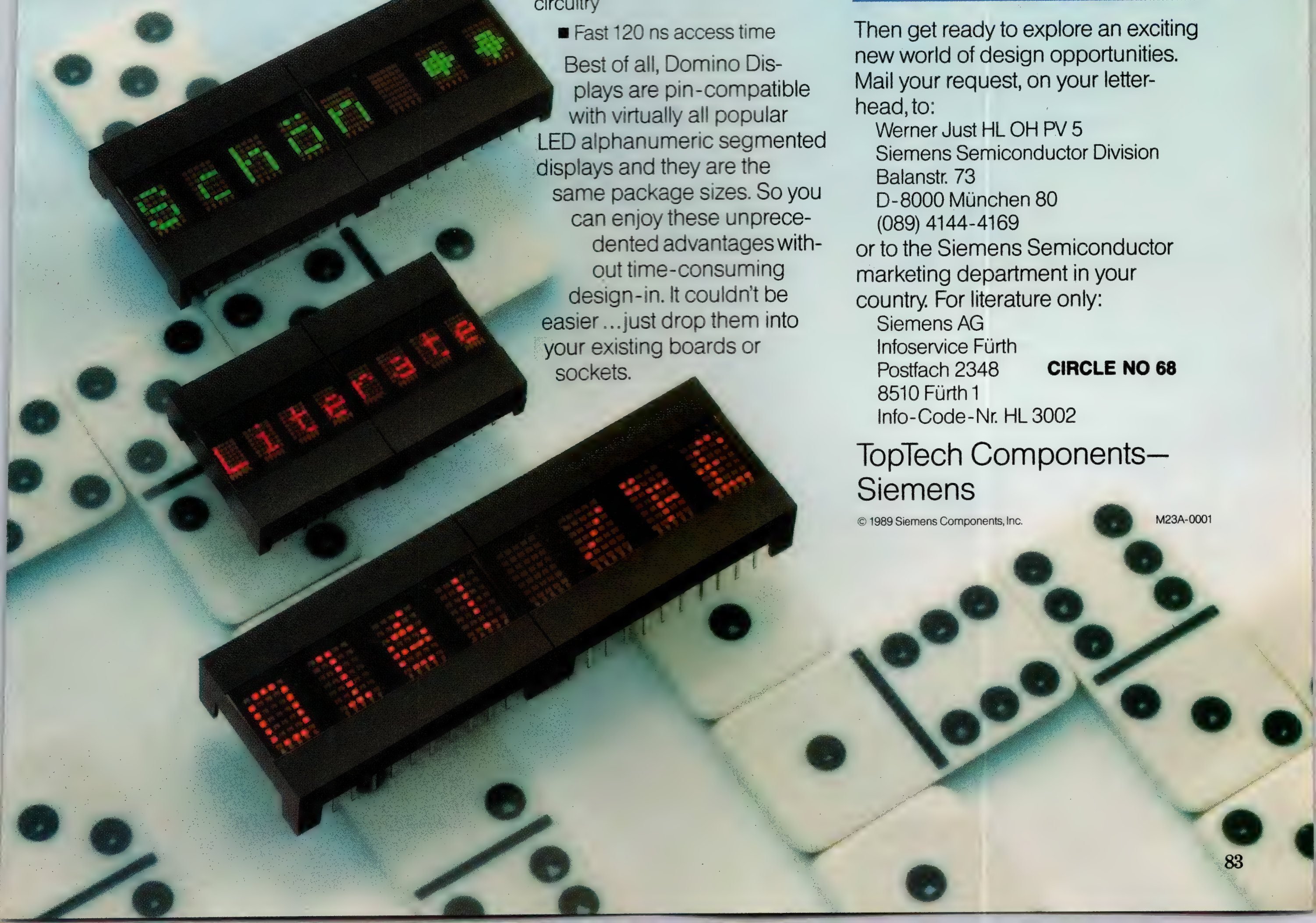

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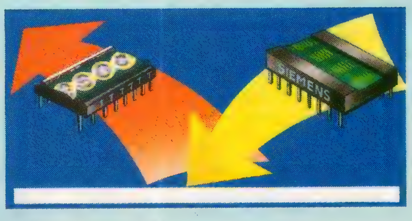

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CIRCLE NO 68

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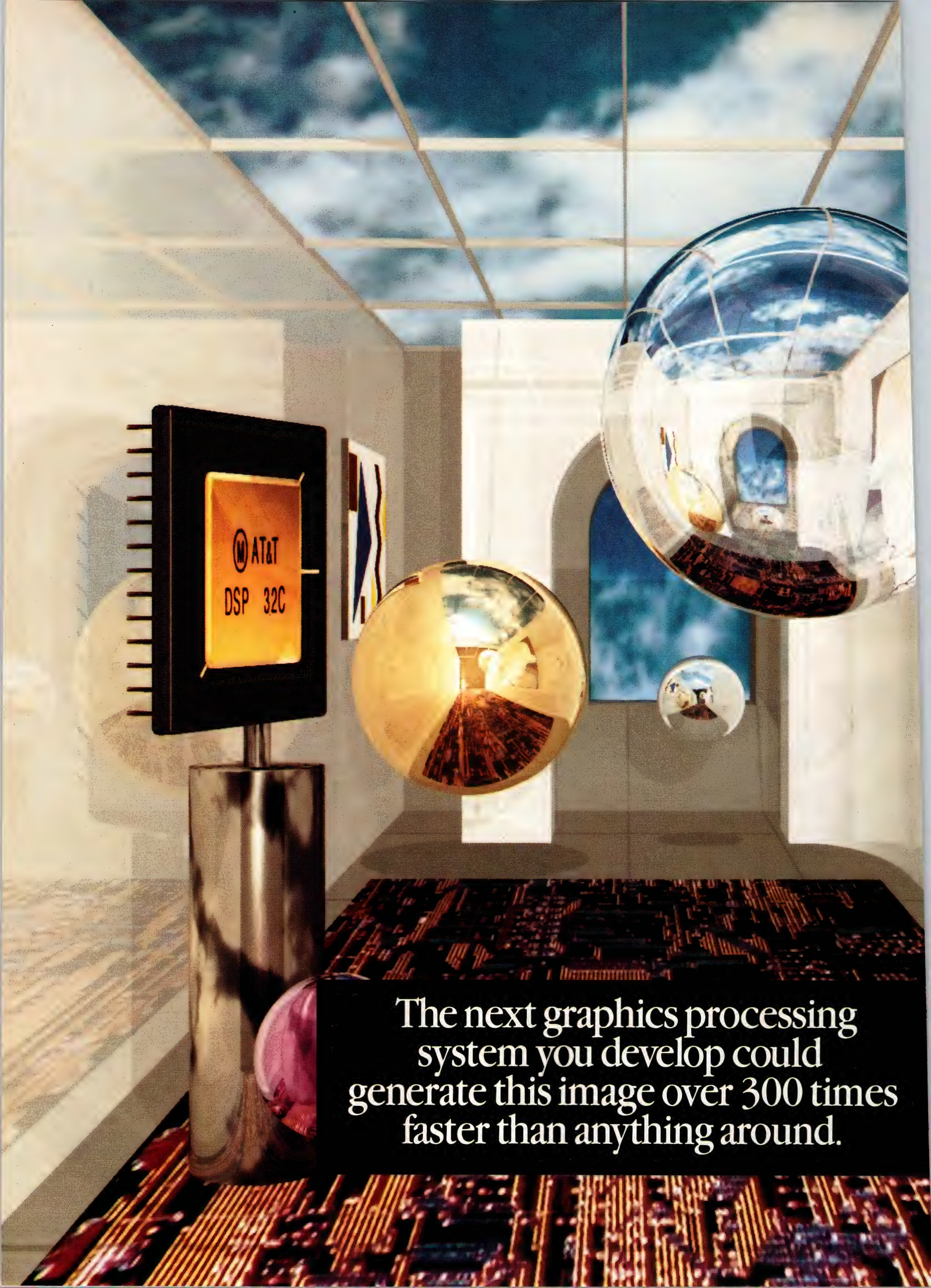
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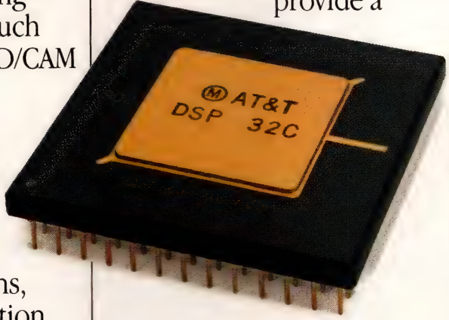

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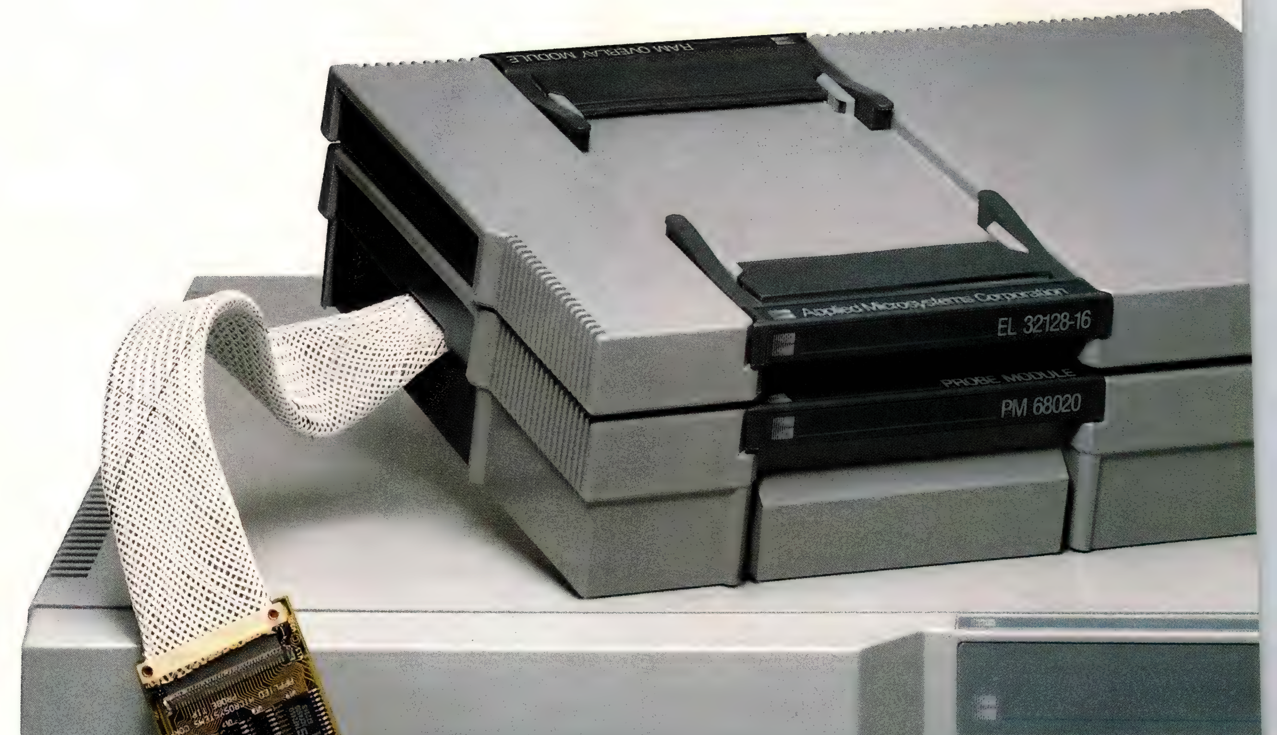
CIRCLE NO 61

FULL SPE



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CIRCLE NO 62

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SG1529	SG3529
Current Mode	
SG1825	SG3825
SG1842	SG3842
SG1843	SG3843
SG1844	SG3844
SG1845	SG3845
SG1846	SG3846
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SILICON GENERAL

CIRCLE NO 63

Portable logic analyzers incorporate dual-channel digitizing scope

Two portable logic analyzers, the HP 1652B and HP 1653B, incorporate a dual- channel digitizing oscilloscope section that allows you to make precision, time-correlated analog and digital signal measurements in addition to performing conventional logic and state analysis. The oscilloscope sections of both instruments feature two channels that digitize signals at rates to 400M samples/sec. The $11,800 HP 1652B and $7900 1653B furnish 80 channels and 32 logic-analysis channels, respectively.

In state-analysis mode, the logic channels of the HP 1652B operate at a maximum rate of 35 MHz, the HP 1653B's logic channels operate at a maximum rate of 25 MHz. Both instruments make timing-analysis measurements at a fixed rate of 100 MHz (recording only when a logic level changes on one or more channels) or at maximum rate of 50 MHz with the instruments' glitch-capture feature enabled. For both logic-analysis modes, the analyzer section stores 1024 samples per channel. The logic-analysis specifications of the HP 1652B duplicates those of the company's recently-upgraded HP 1650B ($7800) logic analyzer, and the HP 1653B specs match those of the company's HP 1651B ($3900) analyzer.

Each of the HP 1652B's and HP 1653B's digitizing oscilloscope channels features 100-MHz single-shot and repetitive bandwidths and digitizes signals at a maximum rate of 400M samples/sec. The instruments store digitized waveforms in independent, 2048-point buffers. Digitization resolution is 6 bits, and the timing accuracy between the two scope channels is better than 1 nsec.

The instruments' digitizing- oscilloscope section can perform several automatic measurements on a captured waveform including pulse width, frequency, period, rise time, fall time, p-p voltage, and overshoot. These automatic measurements reduce the possibility of errors such as those that occur when a bleary-eyed engineer has counted one too many graticule grids too late at night.

By combining a logic analyzer and a dual-channel digital oscilloscope, *the HP 1652B and HP 1653B provide capabilities exceeding those of the equivalent individual instruments.*

If the HP 1652B and 1653B merely combined the functions of a digitizing oscilloscope and a logic analyzer, they would just be space-saving instruments. However, these products link the two instrument sections to provide timing correlations between the oscilloscope and logic-analyzer buffers, and they allow the digitizing oscilloscope and logic analyzer to arm each other's triggers, thus allowing you to make some truly complex measurements.

For example, you can configure the instruments so that the digitizing oscilloscope section arms the logic analyzer. You might use this configuration, for example, to start the capture of digital signals on the clock edge following the point in time when an analog reset voltage, generated by an RC network, reaches a critical threshold voltage. This setup would allow you to study the behavior of a μP-based circuit when power is first applied. Using the oscilloscope section as the trigger element eliminates the chance of false triggering because of unstable logic levels during the power-up sequence.

Similarly, you can use the instruments' logic-analysis section to arm the digitizing oscilloscope's trigger. You might use this configuration, for example, to record the analog signal from the read/write head of a SCSI-based hard-disk drive after the drive receives a command to reposition the head. This measurement cannot be made easily with just a digitizing oscilloscope; traditional digitizing scopes lack the ability to generate a trigger from the complex, multiple-byte, SCSI repositioning command. Because of the time correlation between sections and the combined-triggering features, these two products provide more capability than a simple sum of their two parts might indicate.

—Steven H Leibson

Hewlett-Packard Co, Box 10301, Palo Alto, CA 94303. Phone local office.

Circle No 730

Real-time operating system and tools run on a variety of RISC and CISC µPs

A modular scalable real-time operating system called OS-9000 and a complete native and cross-development tool set supports Motorola 68020, 68030, and 68040 µPs and the Intel 80386 µP. Furthermore, a version for the Intel 80486 µP and the Motorola 88000 RISC processor will be released after the first of the year. You can place all modules of the operating system in ROM, and you can use the operating system for disk- and LAN-based applications as well.

The operating-system kernel can operate in either a timesharing multiuser scheduler mode suitable for a development environment or in a priority-based pre-emptive real-time scheduler mode. The real-time mode features a worst-case interrupt latency of 18 µsecs. The kernel also includes task-synchronization and process-management constructs such as pipes, events, semaphores, and signals.

Memory protection occurs through system state-process permissions, and the operating system can take advantage of standard hardware MMUs (memory management units). The operating system was developed primarily in C for portability and includes a C library interface for I/O operations.

For communications support, you can optionally add the OS-9000/ISP Internet Support Package including drivers that support the TCP/IP (Transmission Control Protocol/Internet Protocol). The company also plans to offer support for ISDN after the first of the year.

The operating system and development tools support development on an OS-9000 native machine, and cross development on Unix systems and on IBM-compatible MS-DOS-based computers. The Unix development tools are available for DEC, Sun, Hewlett-Packard, and Apollo systems. Tools include C, Fortran, and Basic compilers, and a source-level debugger.

Native and cross- development support *and the OS-9000 real-time operating system target applications ranging from ROM-based systems to real-time multiprocessor applications.*

OS-9000 also supports the company's Rave (real time audio/video environment) introduced for OS-9 earlier this year. Developers can use Rave to combine audio, video, computer-generated graphics, and customizable menus in a user interface.

You can expect the company to add support for other RISC (reduced instruction set computer) and CISC (complex instruction set computer) processors in the future. Furthermore, support for multiprocessor architectures is planned for next year. An industrial version of the product that includes the kernel, interprocess communications manager, and I/O manager costs $350. A professional version that adds utility commands, a C compiler, documentation, and 90 days of support costs $650.

— *Maury Wright*

Microware Systems Corp, 1900 NW 114th St, Des Moines, IA 50322. Phone (515) 224-1929. FAX 515-224-1352.

Circle No 731

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CIRCLE NO 64

SIMM memory-packaging technology results in quad-density RAM modules

A new RAM packaging technology, called Flexible Leaded Component (FLC), has resulted in a family of SIMMs (single in-line memory modules) that store four times as much data as industry-standard SIMMs do. For example, a SIMM based on FLC and a 1M-bit dynamic-RAM die stores 4M bytes in the industry-standard 30-pin, 1M-byte package. The technology offers comparable increases in capacity for static-, pseudostatic-, and video-RAM modules.

The FLC makes use of a raw die and is a fully additive semiconductor package. A passivation layer of silicon nitride seals the IC, and a proprietary organic dielectric encapsulates it. Conductive interconnections can be implemented with sputtering or with electroplated metal. A memory module consists of multiple FLC packages.

Initially the technology will be used to produce dynamic-RAM SIMMs. You can now choose from 2M- and 4M-byte offerings compatible with the industry- standard 30-pin SIMM. The 4M-byte DSIMM408-10 and DSIMM409-10 cost $887 and $992 (100), respectively. Both models employ 100-nsec, 1M-byte dynamic- RAM ICs, and the DSIMM409-10 includes a parity bit.

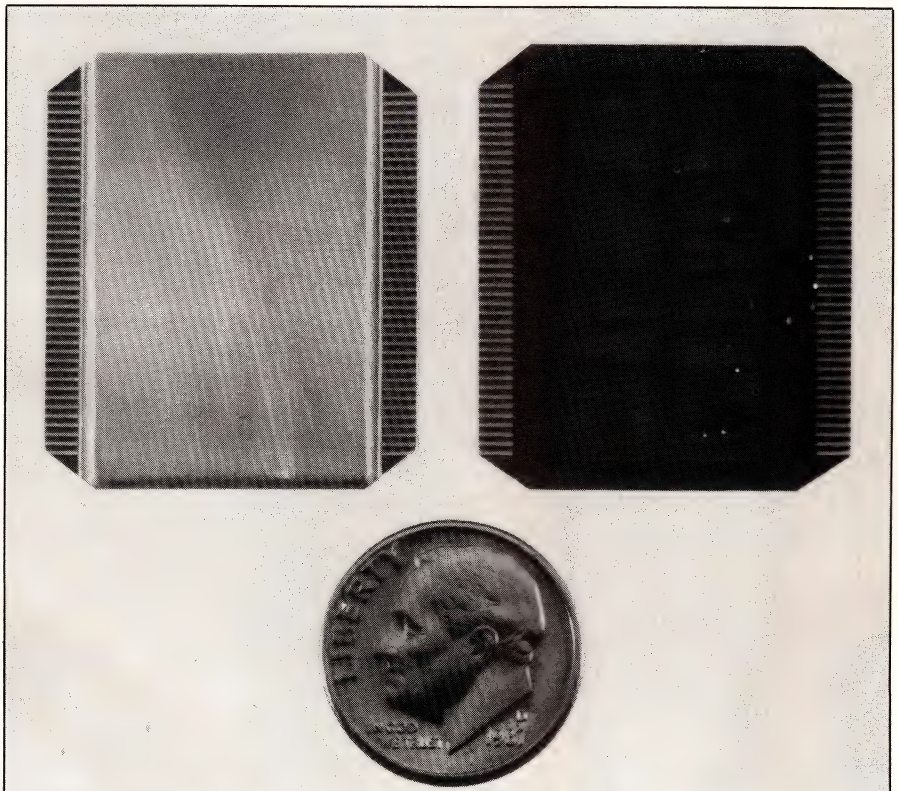
The company also currently offers a 100-nsec, 256k × 16-bit static-RAM module, the SSIMM25616-100, which costs $633 (100) and is byte addressable. No industry standards exist, however, for static-RAM SIMMs. A number of other static-RAM modules are planned, including 64k × 16-bit and 64k × 64-bit products with access-time specs as low as 15 nsec.

Likewise, the company plans to offer modules based on video- and pseudostatic-RAM die. Because of the lack of a variety of SIMM packaging standards, the company expects much of its business for the modules to be on a custom basis. Samples of the dynamic-RAM modules are available now, and once the products reach production stage, the lead time for custom products will only be six weeks.

—*Maury Wright*

Unistructure Inc, 3 Whatney Pl, Irvine, CA 92718. Phone (714) 581-0810.

Circle No 732



Flexible-Leaded-Component packaging technology *is a fully additive semiconductor packaging process that allows memory modules to host four times as many die as industry-standard modules do.*

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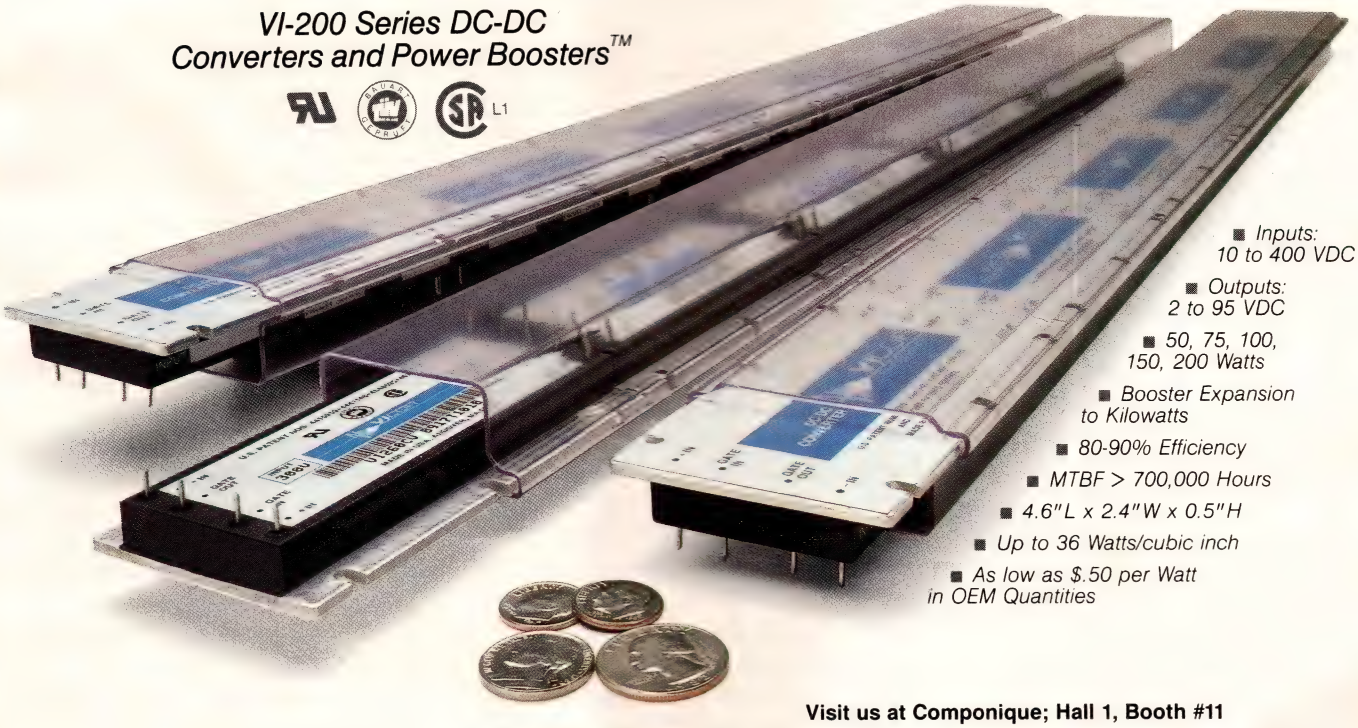

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Cache controller for 80386-based systems handles cache exceptions internally

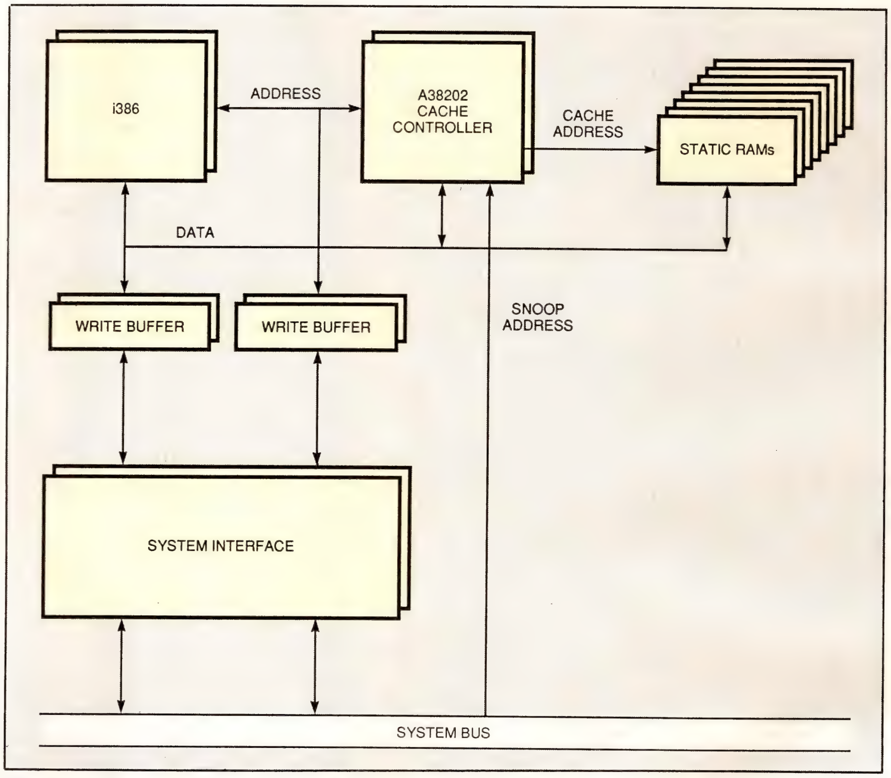
The A38202 cache controller can simplify the task of adding cache memory to your 80386-based system. The device offers a number of features that allow your design to handle coprocessors, noncacheable memory, and memory tests without extra circuitry.

The A38202 connects directly to the 80386 local bus and handles processor clock rates of 25 or 33 MHz. The unit allows you to define a direct-mapped or 2-way set-associative cache using 32k, 64k, or 128k bytes of static RAM. Because the A38202 supports the 80386's pipelined mode, it allows you to use slower SRAM and still achieve zero wait-state cache hits.

To simplify your cache design, the controller allows you to program as many as three regions of memory that are noncacheable. Such regions must be defined for memory-mapped I/O devices and peripherals, for example, where the processor needs access to the actual memory location instead of a copy of its contents. You can further define the internal regions to be noncacheable only on a read or write operation. Thus, you can cache ROM data for read operations without allowing the processor to change the ROM image.

If you need more than three noncacheable regions, the controller accepts signals from external address decoding. You can also disable the cache, making the entire memory noncacheable, with a single software command.

If your system uses a coprocessor, you don't need any extra logic to prevent the cache from reacting to coprocessor calls. The A38202 recognizes attempts to access either the Intel 80387 or Weitek 3167 coprocessor and disables the cache during these operations.



The A38202 cache controller and SRAM are all you need *to build a complete cache for your 80386- based system. The device supports noncacheable regions, coprocessor calls, and bus snooping on chip.*

The A38202 also simplifies the job of maintaining cache coherency by performing asynchronous "bus snooping;" that is, monitoring the system bus to detect writes to main memory from another source, such as a DMA controller. When the cache controller detects such a write operation, it invalidates the cache tag for the address involved, ensuring that the processor will fetch only fresh data. Because the snooping is asynchronous, you don't need to operate your system bus at the processor frequency.

You can easily test your cache memory, using the A38202's diagnostic mode. This mode causes the device to treat the cache RAM as local memory, beginning at x40000, and allowing you to test the cache with the same diagnostic routines you use for main memory. By preloading the cache with a test pattern, you can also run tests to verify the tag-RAM's operation.

The controller comes in a 160-lead quad flatpack and will be available in November. The 33-MHz version costs $98; the 25-MHz version sells for $84 (10,000).

—Richard A Quinnell

Austek Microsystems, 2903 Bunker Hill Lane, Suite 201, Santa Clara, CA 95054. Phone (408) 988-8556. FAX (408) 988-0818.

Circle No 733

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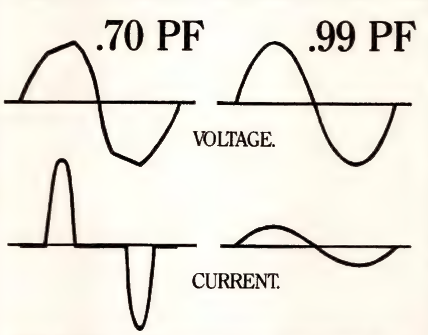

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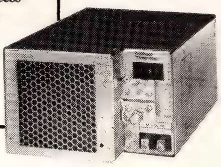

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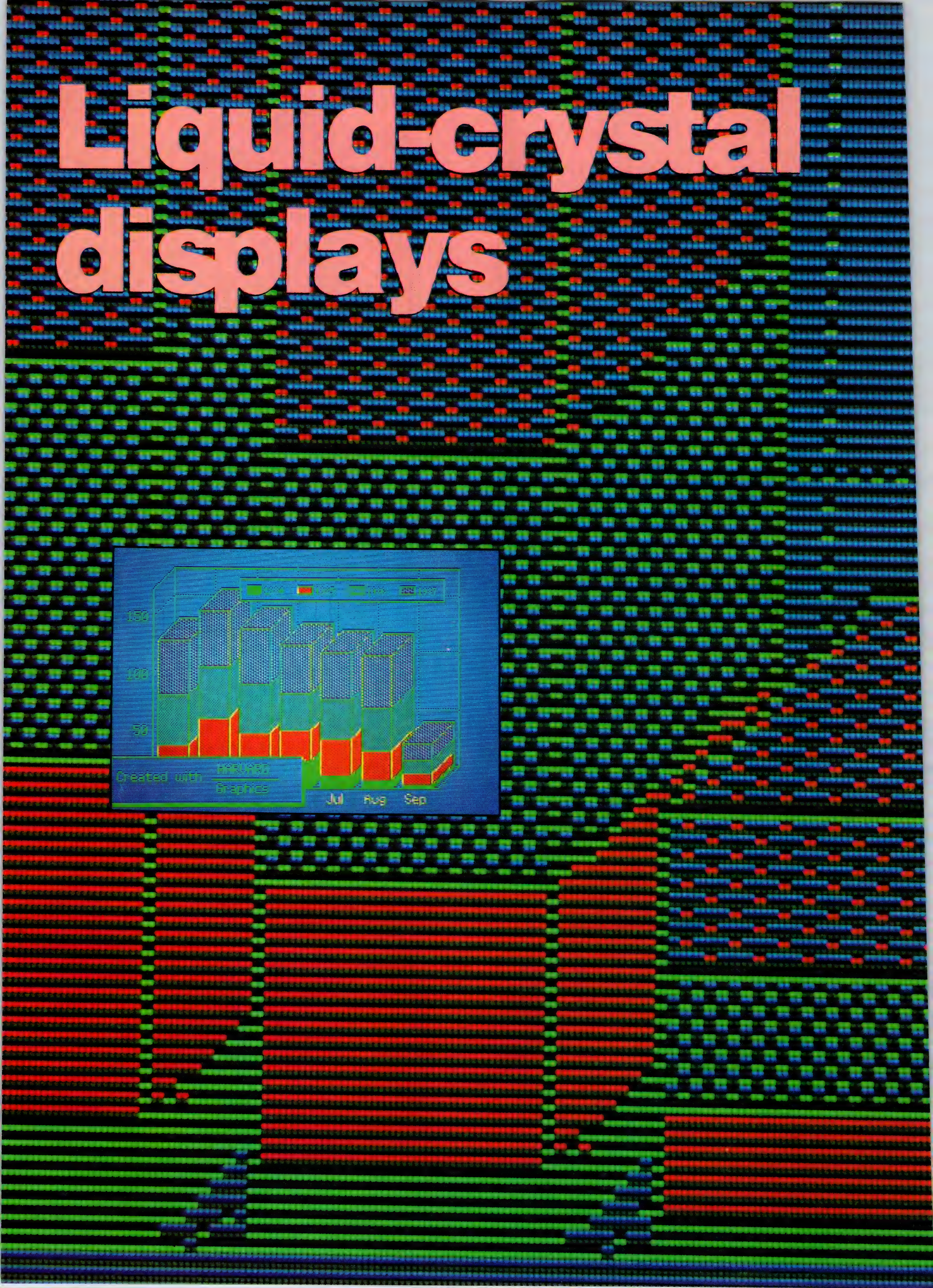
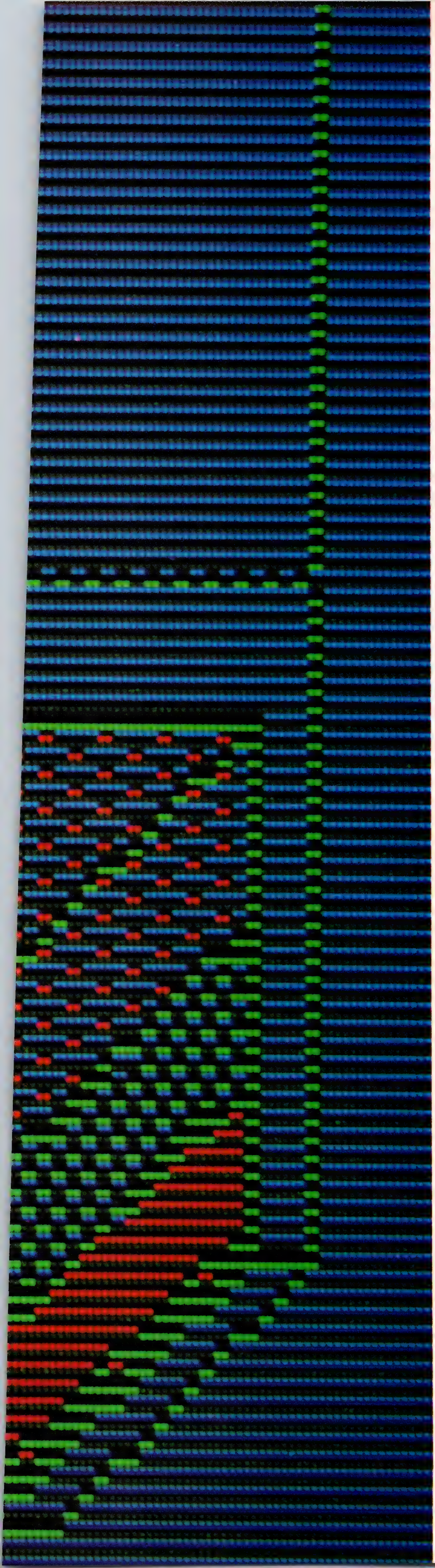
Liquid-crystal displays





EDN SPECIAL REPORT

Liquid-crystal displays (LCDs) continue to change the way people view information. From the ubiquitous 7-segment character displays to the large-area displays used in portable computers, LCDs are making a strong bid to dominate the flat-panel-display market.

Dave Pryce, Associate Editor

In their simplest forms, LCDs offer users many advantages. They are inexpensive, thin, durable, and lightweight, and they consume very little power. Their major disadvantages have been poor contrast, low brightness, and a narrow viewing angle. Until a few years ago, these disadvantages restricted the use of LCDs to low-performance applications such as digital watches and calculators, simple alphanumeric displays, and inexpensive laptop computers.

But this situation is changing. Improved technologies such as supertwist, double supertwist, and thin-film transistors have not only greatly improved the contrast and viewing angle of simple displays but have also expanded the application base for LCDs. Large-area displays utilizing these technologies are suitable for high-performance computers and video-graphics terminals. Large-area color LCDs are also becoming available and, together with their monochrome siblings, are making a strong bid to replace other types of flat-panel displays and, ultimately, the cathode-ray tube.

Before reviewing some of the available products, it's instructive to look at the newer technologies that are instrumental in achieving the vastly improved performance of today's liquid-crystal displays. **Fig 1** illustrates four of the possible constructions of LCDs **(Ref 1)**. In the basic twisted-nematic display **(Fig 1a)**, indium tin oxide deposited on the inside of each glass plate forms row and column electrodes. Because the buffed front glass is perpendicular to the buffed rear glass, the

***Large-area, color, liquid-crystal displays** are suitable for high-performance applications such as computers and video-graphics terminals. (Photo courtesy Hitachi America Ltd. The magnified pixel arrangement was achieved using an Hitachi color thin-film-transistor liquid-crystal display and Harvard Graphics^{TM} CGA technology. Harvard Graphics is published by Software Publishing Corp (Mountain View, CA).)*

Although still used in low-cost applications, the basic twisted-nematic LCD suffers from two disadvantages: low contrast and a narrow viewing angle.

liquid-crystal layer imposes a 90° rotation, or twist, on the plane of polarized light passing through the display. In the off state, only the vertically oriented components of the unpolarized light can pass through the front polarizer. The 90°-rotated plane of polarized light then exits through the rear polarizer, which results in a lighted pixel.

Applying a low voltage to a twisted-nematic display's electrodes causes an electric field to develop in the liquid-crystal layer. In this on state, the liquid-crystal molecules align themselves in a direction parallel to that of the electric field. Because the plane of polarization isn't rotated, the rear polarizer absorbs the light. The result of this action is a black pixel, which is defined by the intersecting electrodes, on an illuminated background. Reflective and transflective displays, which depend on ambient light for operation, use a reflector layer as part of the display. Transmissive displays, which depend exclusively on backlighting for illumination, do not use a reflector.

Although the conventional twisted-nematic LCD is still used in low-cost applications, it suffers from two major disadvantages: a contrast ratio of less than 3:1 and a viewing angle of less than ±20°. For direct-addressing applications and multiplexed operation with a limited number of lines, these LCDs perform reasonably well. However, for applications in which displays must handle a lot of information, the poor contrast of twisted-nematic displays usually render them unsatisfactory. Enter the supertwist display.

A modified transmission-voltage characteristic gives the supertwist LCD a higher multiplexing rate for a given contrast ratio. This display rotates the plane of polarization between 180 and 270°. In addition, alignment layers in the display provide a pretilt of 10 to 20°. This increased twist and pretwist give supertwist displays contrast ratios as high as 10:1 and viewing angles as high as ±40°. Despite this improved performance, these displays suffer from two disadvantages. The first is the limited ability of supertwist displays to render gray scale, which is caused by their steep transmission characteristic. The second disadvantage results from a birefringent effect, which produces either black figures on a yellow background or white figures on a blue background, depending on the orientation of the polarizers. Many users prefer a black-and-

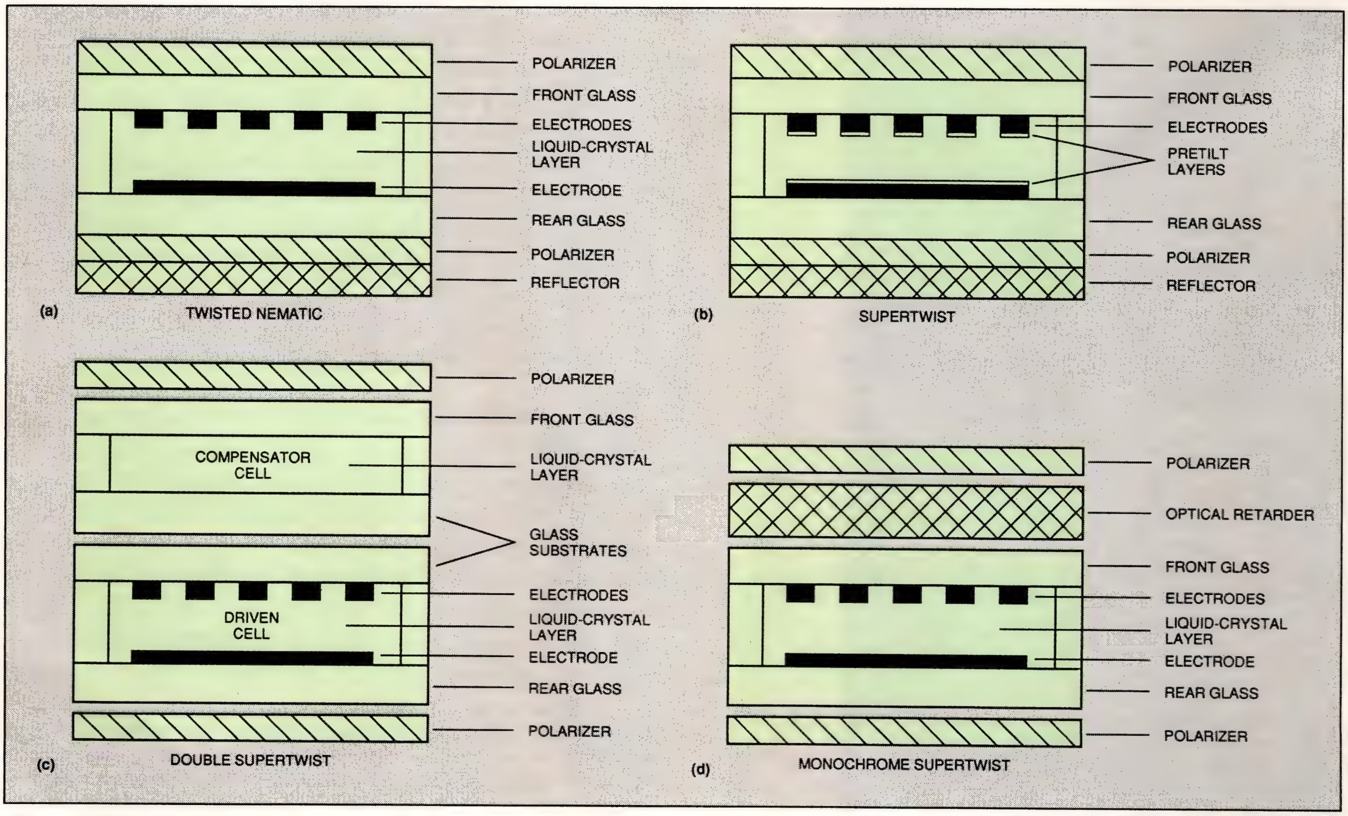


Fig 1—LCDs are available in a variety of technologies. *Four common constructions are twisted nematic **(a)**, supertwist **(b)**, double supertwist **(c)**, and monochrome supertwist **(d)**.*

white display and find the characteristic blue tinge of supertwist displays unacceptable. Enter the double-supertwist display.

The double-supertwist display (**Fig 1c**) includes a color-compensating cell in addition to the standard supertwist cell. The front cell only functions as an optical compensator—it is not electrically driven. Because the optical axes of the compensator cell and the driven cell are perpendicular to each other and their direction of twist is opposite, the double-supertwist display cancels any birefringence colors. The result is an almost pure black-and-white image. In addition, the double-supertwist display has almost twice the contrast of a supertwist display and a somewhat wider viewing angle of about ±45°. The main disadvantage of a double-supertwist LCD is its need for a high-power fluorescent backlight to overcome the transmission losses caused by the addition of the compensator cell. By contrast, a supertwist display can use a low-power electroluminescent backlight. Because of its more complex assembly, the double-supertwist display is also more expensive than a supertwist display.

To overcome the higher cost of the double-supertwist display while maintaining its improved contrast and viewing angle, manufacturers developed the monochrome supertwist display. This display (**Fig 1d**) consists of a supertwist LCD and an optical-retarder layer positioned between the front polarizer and the front glass. Made from an inexpensive polymer material, the optical retarder replaces the expensive compensator cell of the double-supertwist display. One problem with the monochrome supertwist display, however, is controlling the exact thickness of the multilayer polymer material.

Supertwist, double-supertwist, and monochrome supertwist technologies are important developments in the effort to improve the contrast and viewing angle of LCDs, and manufacturers continue to explore other technologies for displays capable of handling large quantities of information at high data rates. Until recently, high-resolution displays capable of reproducing CGA, EGA, and VGA standards were the exclusive province of the CRT. Although plasma and electroluminescent displays have been used in high-resolution portable computers, they don't offer the low-power advantage of LCDs. Moreover, the plasma display exhibits particularly poor contrast—at least to the human eye—because of its characteristic orange-on-black color. To answer the need for high contrast and high resolution, manufacturers of large-area LCDs have turned to active-matrix, thin-film transistor technology and continue to improve double-supertwist technology.

The active-matrix LCD uses an array of thin-film

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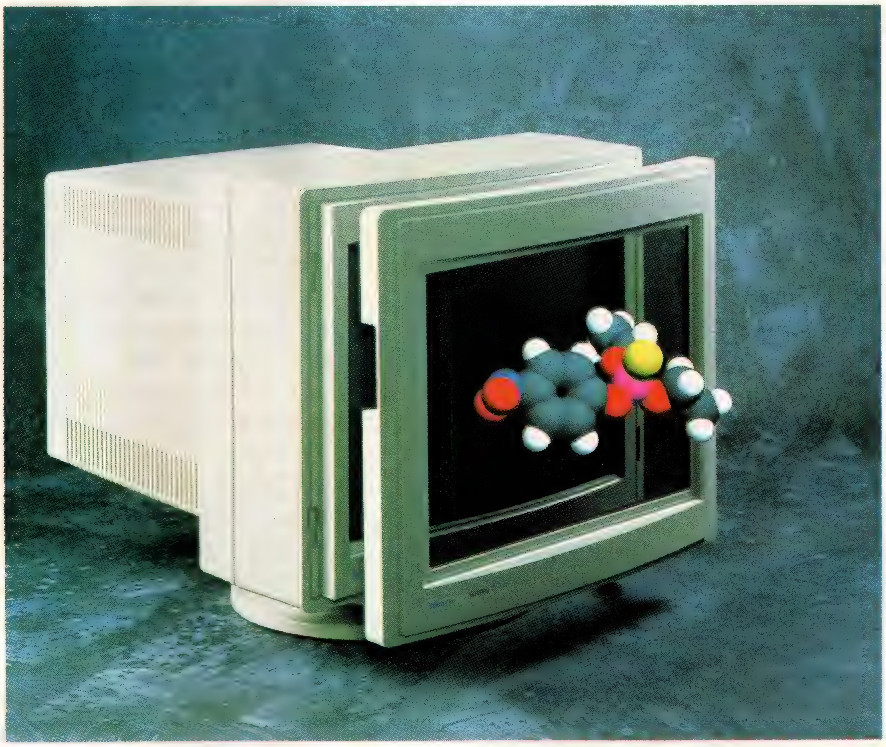


A radical departure from the typical LCD panel, *this liquid-crystal modulator panel mates with a 19-in. color monitor to provide 3-D stereoscopic viewing. Available from Tektronix, the SGS-625 system has a resolution of 1280 pixels × 1024 lines.*

A glossary of liquid-crystal-display terms

Acuity—The uniformity of light emission across a pixel and its degree of edge definition. Assuming the contrast ratio is high enough for the easy distinction of on and off pixels, the emission uniformity of the on pixels, together with the size and shape of the pixels, dictates the sharpness of the images.

Aspect ratio—The ratio of the display's width to its height. An aspect ratio of 4:3 is typical for a TV screen or computer monitor. LCDs come in a variety of aspect ratios, depending on the particular application.

Backlighting—Used in transflective and transmissive displays to provide most or all of the screen's brightness. The bulb or bulbs are usually mounted on the back of an LCD panel but are sometimes mounted on the sides of the display. Several types of bulbs are used for backlighting, including cold-cathode fluorescent, hot-cathode fluorescent, and electroluminescent types.

Birefringence—The splitting of a light beam into two light waves as the beam passes through a crystal. The resultant two light waves vibrate in directions that are perpendicular to each other. Most liquid-crystal material exhibits birefringent properties. Because the phase difference between the two waves depends on their wavelengths, a color change may result from birefringence. This color change depends on the orientation of the display's polarizing elements.

Brightness—The light intensity, or luminosity, of the display. Brightness is measured in foot lamberts (fL) or in candelas per square meter (cd/m^2). Note: 1 cd/m^2 = 0.292 fL.

CGA—Color-graphics adapter. An electronic display standard that specifies a resolution of 640 × 200 pixels in the 2-color mode and 320 × 200 pixels in the 4-color mode from a palette of 16 colors. The horizontal scanning frequency is 15.75 kHz.

Contrast ratio—The ratio of on-pixel brightness to off-pixel brightness. Contrast is basically the difference in light intensity between the foreground and background of a display. Black and white provide the ideal contrast. Contrast ratios for LCDs range from less than 3:1 for a simple twisted-nematic display to as high as 40:1 for an active-matrix display with thin-film transistors. Although the perceived contrast depends on the ambient light, a contrast ratio of about 7:1 is generally considered acceptable. Above a ratio of about 15:1, the human eye perceives little difference in contrast.

Controller—A pc board that goes behind the display or in the computer bus. The controller lets the computer communicate with the display. For a CRT raster-scan display, the controller provides the signals needed for horizontal synchronization, vertical synchronization, and serial data. Flat-panel displays, such as LCDs, usually require an additional signal—the dot-clock signal—to control the transfer speed of the pixel information.

Display size—The illuminated area of the display that is available for viewing data. CRTs are usually specified according to their diagonal measurement. Flat-panel displays, such as LCDs, are usually specified according to their height and width.

Dot—See ***Pixel.***

Dot-clock signal—The signal that controls the pixel rate for the display system. Digital technologies, such as flat-panel displays, require this signal to tell the host system how fast to read the individual pixel information from the system to the panel. Analog CRT displays don't require this signal.

Double-supertwist LCD—Similar to the supertwist LCD, the double-supertwist display adds a color-compensating glass substrate to provide an almost pure black-and-white image. A double-supertwist display has nearly double the contrast of a supertwist display and a somewhat wider viewing angle of about ±45°. The main disadvantage of a double-supertwist LCD is its need for a high-power fluorescent backlight to compensate for transmission losses caused by the added layer. By contrast, the supertwist display can use a low-power, electroluminescent backlight.

Duty cycle—The amount of time it takes for an electronic display to refresh every pixel on the screen. The maximum acceptable time is about 16.6 msec, which corresponds to a minimum refresh rate of 60 Hz. At refresh rates slower than about 60 Hz, the human eye begins to detect a flicker in the display.

EGA—Enhanced-graphics adapter. An electronic display standard that specifies a resolution of 640 × 350 pixels with 16-color capability from a palette of 64 colors. Included in this standard are 40- and 80-column text modes and CGA emulation.

Fill factor—The percentage of the total area of the display that is illuminated at any given time. Displays with a fill factor of 20% tend to look like a collection of dots. Displays with fill factors of 50% or more exhibit greater apparent brightness and are generally more readable and aesthetically pleasing.

Film-supertwist LCD—Similar to a double-supertwist display except for the replacement of one of the optical-compensating glass layers with an ultrathin polymer film. Compared with double-supertwist displays, the film-supertwist display has slightly less contrast but offers significant advantages, including a viewing angle as high as ±60° and low-power electroluminescent backlighting.

Flat-panel display—An electronic display with a package thickness that is a fraction of the display's height or length. Package thickness varies from about 0.5 to 2.5 in. The pc board containing the electronics sometimes accounts for a significant portion of the total thickness.

LCD—Liquid-crystal display. These displays are made from liquid materials obtained from certain organic solids. The liquid molecules exhibit an ordered structure as well as freedom of movement. In a twisted-nematic display, a liquid-crystal mixture is sandwiched between two glass plates that are coated with a polarizer and lined with transparent electrodes. The application of an electric field shifts the nematic molecules so that they line up with the field, thus changing the display's optical characteristics.

Monochrome-supertwist LCD—Similar to the double-supertwist display, the monochrome-supertwist display replaces the expensive compensator cell of the double-supertwist LCD with an optical retarder made from a less expensive polymer material. Both LCDs feature a high-contrast black-and-white display and a wide viewing angle.

Nematic—Threadlike, the typical shape of a liquid-crystal molecule.

Pixel—A picture element. The smallest unit of a video display. The term *pixel* is commonly associated with a CRT. For dot-matrix LCDs, the term *dot* is more commonly used.

Reflective display—An LCD that depends entirely on ambient light for illumination—it has no backlighting. Reflective displays, which are best suited for positive images, contain a rear reflector and perform best under strong lighting conditions.

Resolution—The quality and sharpness of a display. A number of factors determine the real or apparent resolution of a display. These factors include the pixel or dot size and pitch, the number of lines per inch, and the total number of pixels. The best quantitative measurement of resolution is probably the total pixel count in a given area.

Supertwist LCD—A liquid-crystal display that rotates the plane of polarization between 180 and 270°. A conventional twisted-nematic display imposes only a 90° twist on the plane of polarized light passing through the display. In addition, an alignment layer in a supertwist display provides a pretilt of 10 to 20°. The pretilt and increased twist give supertwist LCDs contrast ratios as high as 10:1 and viewing angles as high as ±40°. Despite the improved contrast and viewing angle, many people find the characteristic blue tinge of a supertwist LCD unacceptable.

Thin-film-transistor LCD—A twisted-nematic display that incorporates an active matrix of thin-film transistors to control the turn-on and -off of each pixel. These displays can achieve a viewing angle greater than ±45°, a contrast ratio of 40:1, and response times as fast as 40 msec. By including red, blue, and green filters over each pixel, a thin-film-transistor LCD can reproduce an 8-color image. The main disadvantage of these state-of-the-art displays is their high cost, which is due to manufacturing complexities.

Transflective display—An LCD that operates under ambient light or with backlighting. As the name implies, a transflective display is a compromise between the transmissive and reflective types. Used in the reflection mode, the display is not as bright and has lower contrast than reflective types. Transflective displays are most appropriate in applications in which they must operate in a wide range of indoor and outdoor lighting conditions.

Transmissive display—An LCD that does not incorporate a reflecting rear surface—it must be backlit continuously when in use. Transmissive LCDs, which are best suited for negative images (light segments on a dark background), are used in applications in which the ambient light is low.

Twisted-nematic LCD—A display in which the liquid-crystal material imposes a 90° rotation, or twist, on the plane of polarized light passing through the display. Conventional twisted-nematic LCDs have contrast ratios of less than 3:1 when viewed head-on and exhibit a viewing angle of less than ±20°.

VGA—Video graphics array. An electronic display standard that specifies a resolution of 640×480 pixels with 16-color capability and 320×200 pixels with 256-color capability from a palette of 256k colors.

Viewing angle—The range at which you can view a display, measured in angular degrees from a plane that is perpendicular to the display's surface. A viewing angle of ±45°, for example, lets you view a display at any angle from 0 to 45° from the perpendicular. A conical viewing angle provides a view from above, below, or either side of the display.

Advances are improving the performance of simple displays and extending the use of large-area LCDs to high-performance graphics uses.

transistors, which are an intrinsic part of the display. An individual transistor drives each pixel in the display. The tran-sistors are usually FET devices made from amorphous silicon or, in some cases, polycrystalline silicon. Each pixel in the display is isolated from the matrix by this thin-film transistor, which is addressed by the row and column drivers. Although the interface circuitry for the display is multiplexed, each pixel is statically driven by the individual thin-film-transistor drive circuit. This approach preserves the simplicity of a multiplexed display and, at the same time, minimizes the resolution/contrast tradeoff associated with other LCD technologies.

Fig 2 illustrates the basic arrangement of an active matrix using thin-film transistors. In this circuit, the drain leads of the FETs are connected to form column-selecting terminals, and the gate leads are connected to form row-selecting terminals. When the applied row-column signals select a particular pair of row-column terminals, that individual FET turns on, activating the LCD pixel connected to that FET's source lead. In this example, which shows only four of possibly several hundred-thousand pixels, two pixels are turned on and two pixels are turned off.

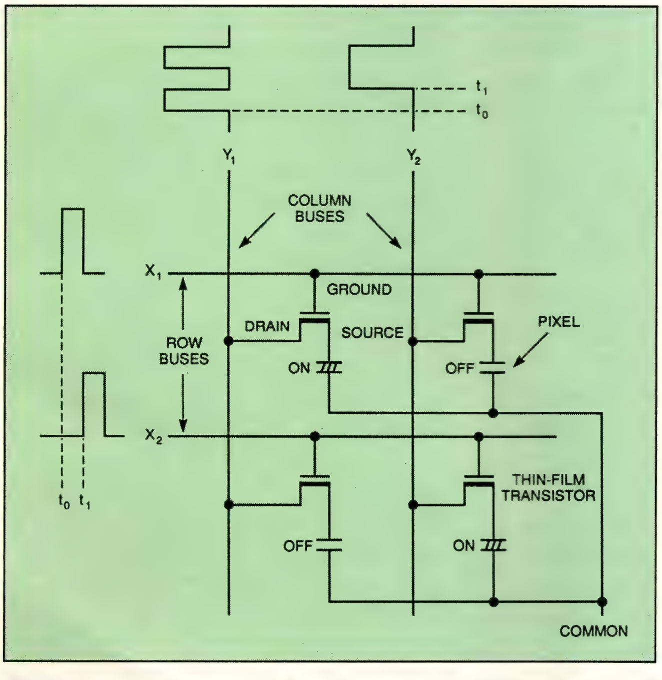
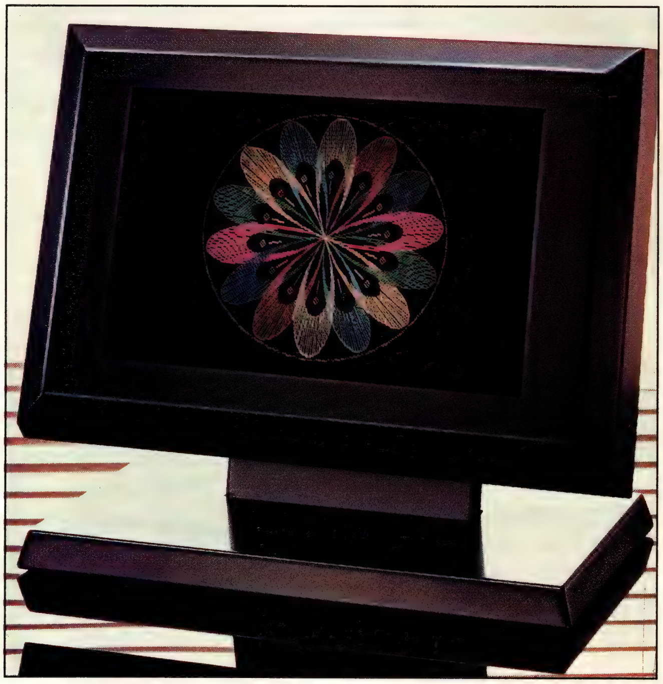


Fig 2—In an active-matrix thin-film-transistor display, *each pixel is driven by its own transistor. The thin-film transistors are usually FETs in which the drain leads are connected to form column-selecting terminals and the gate leads are connected to form row-selecting terminals.*



This 6.3-in., 8-color display *from Hitachi uses thin-film-transistor technology to achieve state-of-the-art performance. The LCD features a resolution of 640×(200×3) pixels, a contrast ratio of 40:1, and a response time of 40 msec.*

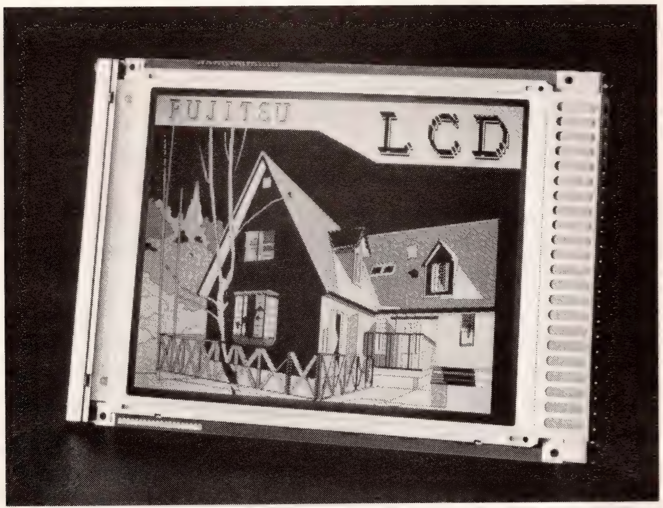
Although the high cost of producing active-matrix LCDs containing hundreds of thousands of individual transistors is now a major obstacle to the acceptance of the thin-film-transistor display as a replacement for the CRT, this acceptance will eventually take place in power-sensitive applications and where size and weight are important considerations. Manufacturers should eventually achieve satisfactory yields with the complex thin-film-transistor technology and thus reduce selling prices to a level that is acceptable for a wide range of applications. Present-day yields, however, preclude the possibility of significant short-term price reductions. A state-of-the-art device from the Electron Tube Division of Hitachi America illustrates the problem.

With a selling price of about $680 for a monochrome display and $700 for a color display in OEM quantities, Hitachi's 384,000-pixel thin-film-transistor display is certainly a leading-edge product, but its high cost is a major deterrent for many applications. It should, however, be of interest to manufacturers of avionics displays, medical-imaging equipment, and high-end laptop computers. And, when yields improve and costs are lowered, displays of this type are likely to dominate many other applications.

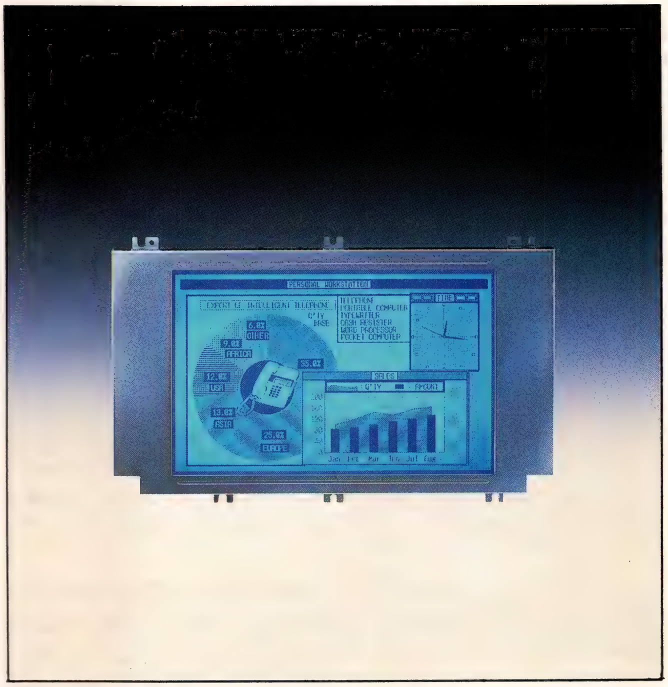
With an effective display area of about 19 in.^{2}, this Hitachi 6.3-in. (diagonal), 8-color LCD module has some impressive specs. Its resolution is 640×(200×3) pixels for color versions and 640×600 pixels for monochrome versions. The dot, or pixel, pitch is a sharp 0.16×0.20 mm with the pixels arranged in horizontal stripes. The display also features a contrast ratio of 40:1; a typical response time of 40 msec, which makes the display suitable for mouse-driven applications; and a viewing angle of ±45°. The module, which operates from 5 and 25V dc supplies, consumes only 1.5W. Transmissive in nature, the display also requires a fluorescent backlight, which consumes an additional 3.5W.

A display for the truly affluent

If a sample price of $16,460 won't seriously dent your bank account, you might want to take a look at another state-of-the-art display. Of interest primarily to the military and avionics industries, the AM-6448 from Ovonic Imaging Systems is an active-matrix display with a 6×8-in. (10-in. diagonal) viewing area and a resolution of 640×480 pixels. Compared with the previously mentioned Hitachi display, the AM-6448 offers a much larger viewing area but is available only in a black-and-white version. The Ovonic display also differs in the design of its active matrix. Rather than using thin-film transistors, each of the display's 307,200 pixels is driven by a semiconductor switch consisting of amorphous silicon diodes.



Using double-supertwist technology, *this LCD panel from Fujitsu Components has a viewing area of 8.3×6.2 in. The display, which uses cold-cathode fluorescent sidelighting, has a resolution of 640×480 pixels.*

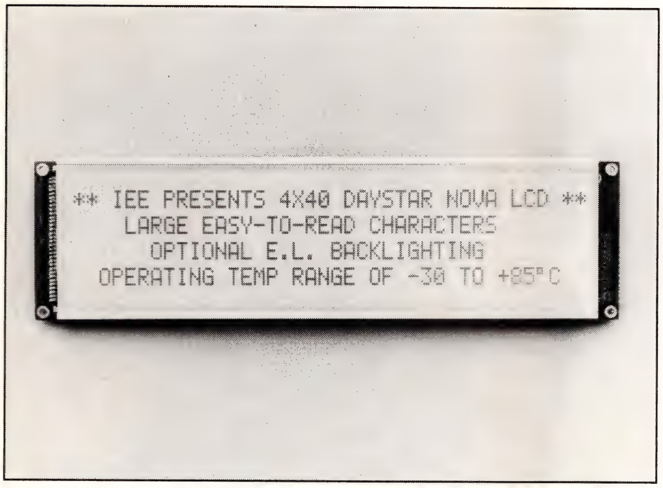


With an overall size of 11.8×6.5×0.9 in., *this LCD from Sharp Electronics uses blue-negative-mode supertwist technology. The display has a high contrast and a resolution of 640×400 dots.*

Ovonic Imaging Systems has a convincing argument for its use of diodes in the display's active matrix. With diodes, the horizontal and vertical conductors of the dot matrix are not on the same glass substrate. This isolation eliminates the need for insulated crossovers, which are a principal source of line defects in active-matrix displays. Moreover, the series arrangement of diodes in each switch provides redundancy against shorts, thereby minimizing individual pixel defects. The AM-6448 was originally developed as a transflective display, with a thin fluorescent backlight providing illumination for dim-light conditions. The AM-6448 is also available as a reflective or transmissive display. You can introduce color through the use of filters, which result in solid-color or multicolor displays.

In addition to its large viewing area and high resolution, the AM-6448 features a contrast ratio of 20:1 and viewing angles of ±70° horizontally and +10 to −45° vertically. Power consumption is less than 2.2W, but the addition of a backlight raises this spec to nearly 12W. Although the display is impressive in its clarity and definition, its astronomical selling price limits its use to applications that are not cost sensitive. Ovonic Imaging Systems reports high yields with the AM-6448

New technologies such as supertwist and double supertwist provide contrast ratios as high as 20:1 and viewing angles greater than ±40°.


** IEE PRESENTS 4X40 DAYSTAR NOVA LCD **
LARGE EASY-TO-READ CHARACTERS
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OPERATING TEMP RANGE OF -30 TO +85°C

Typical of alphanumeric dot-matrix displays, *this large-character LCD module from IEE can display four lines of 40 characters each.*

display, but the company's limited production capacity does not allow enough volume to reduce the selling price to a level acceptable to the commercial market. And, its pockets are not yet deep enough to expand its production facilities. But with high-volume production, Ovonic Imaging Systems claims it could reduce the OEM price of the display to less than $500.

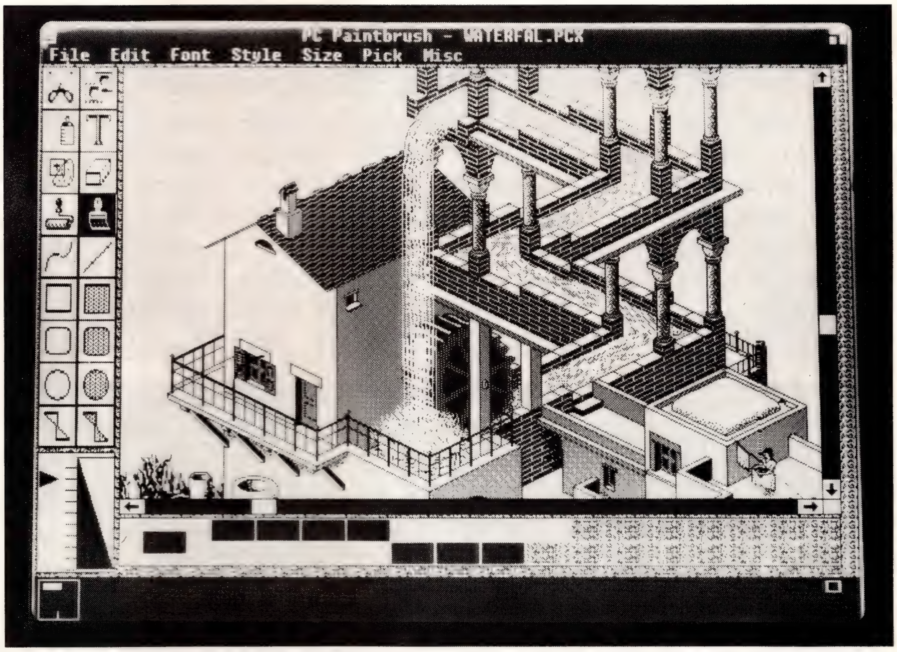
Returning to the more commercially affordable displays, a 10-in.-diagonal black-and-white unit from Hitachi uses double-supertwist technology. Featuring a paper-white image quality, the display has a VGA resolution of 640×480 pixels, a 0.33×0.33-mm dot pitch, a contrast ratio of 20:1, and a viewing angle of ±40°. Because it can provide 16-level gray scaling, the LCD can display color graphics images in monochrome. The display is less than 1 in. thick and, with a cold-cathode fluorescent backlight, consumes less than 7W of power. Priced at $650 in sample quantities (OEM prices are substantially lower), this display should find ready application in high-end laptop computers requiring high-contrast VGA graphics. Hitachi is also developing a 10-in. color LCD using thin-film-transistor technology that it expects to announce in the near future.

Sharp Electronics, probably the world leader in the production of large LCDs, offers a wide range of displays including supertwist and double-supertwist types. The company is also active in the development of large-area, color, thin-film-transistor displays and expects to announce products by early 1990. Sharp, which owns the basic patent on double-supertwist technology, offers one of the largest panels of this type yet available. Its 640×480×3-dot RGB (red-green-blue) color display has an 11×8.2-in. viewing area with a diagonal measurement of about 14 in. This 921,600-pixel display is priced at just under $1000 in small quantities and is capable of reproducing 256 colors. Based on paper-white double-supertwist technology, the display features a 0.145-mm pixel pitch, 8 lines/mm of resolution, and a 15:1 contrast ratio. Due to its large size, the display is particularly well suited for use as a monitor in computers and video terminals. In these applications, the display's somewhat limited viewing angle of about ±20° vertically and ±25° horizontally is not a major problem.

Another large-area display from Sharp is the LM64135T, a blue-negative-mode supertwist display with a 640×400-dot resolution. According to the company, this display, which employs proprietary liquid-crystal material and polarizers, achieves a 200% improvement in contrast at 50% the packaging density of conventional supertwist displays. Its overall dimensions are 11.8×6.5×0.9 in. The display, which has a sample price of $351, features white graphics on a blue background and comes with a built-in cold-cathode fluorescent backlight.

Exploiting the advantages of monochrome-supertwist technology, Toshiba Components recently introduced a pair of these high-contrast, black-and-white displays. Designed for use in laptop computers, workstations, and word processors, the displays feature a contrast ratio greater than 12:1 and a detachable fluorescent backlight. The TLX-1501 has a resolution of 640×400 pixels and a dot pitch of 0.33×0.33 mm. The horizontally oriented display has overall width×height×depth dimensions of 12.6×7.77×0.86 in. The other display, the TLX-1551, has a somewhat greater resolution of 640×480 pixels and a slightly finer dot pitch of 0.31×0.31 mm. The TLX-1551 is vertically oriented and has overall dimensions of 7.16×10.86×0.86 in. In sample quantities, these Toshiba displays cost $646 and $720, respectively.

Perhaps better known as a major supplier of plasma displays, Fujitsu Components also offers several liquid-crystal displays that qualify as large-area types. Its FLC640-480WSUB, for example, has an 8.3×6.2-in. viewing area with a typical brightness of 15 fL and a 15:1 contrast ratio. Using transmissive double-supertwist technology, the display features a 640×480-pixel resolution and a 50° viewing cone. To achieve optimum viewing, the designers of the display used a computer simulation program to determine the dot patterns and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This high-performance display uses thin-film diodes in an active matrix. *Available from Ovonic Imaging Systems, this expensive display features a viewing area of 6×8 in., a VGA resolution of 640×480 pixels, a contrast ratio of greater than 20:1, and a total viewing angle of 140°.*

locations for each 0.30×0.30-mm pixel. In addition, Fujitsu developed special circuitry that virtually eliminates undesirable crosstalk—a phenomenon that occurs when selected pixels merge into unselected pixels to produce streaks of light. The $575 (1000) display also uses custom-designed, side-mounted, cold-cathode-fluorescent bulbs to reduce the display's thickness to 0.8 in.

Seiko is well known for its high-quality watches, which use 7-segment LCDs to display the time and date. The company also has a division that offers a wide range of dot-matrix LCD modules. Included in Seiko Instruments' product line are several large-area types. For example, its G642GX5*000 panel features a viewing area of 8.6×6.6 in. (10.8 in. diagonal) with a resolution of 640×480 pixels. Called a Super New TN (SNTN) display by the company, the module is basically a film-supertwist type that uses Seiko's RCF (Retardation Compensation Film) technology to neutralize chromaticity and thereby yield a black-and-white display. The display, which has a gray-scale capability of at least eight levels, uses side-mounted lighting to reduce the panel thickness to less than 0.6 in. Power consumption for both the display and backlight is less than 3W, a spec that is about half that of other similar-sized modules. In sample quantities, the display costs $500.

Another company better known for products other than its liquid-crystal displays is Epson America Inc. Well known for its line of printers and personal computers, Epson also makes LCDs. Its EG-9001 and EG-9002 panels are representative of its large-area types. Although both the EG-9001 and EG-9002 have a viewing area of 8.3×6.2 in. (10.3 in. diagonal) and a resolution of 640×480 pixels, they differ in other respects.

The EG-9001 displays black characters on a white background using a double-layered, supertwist technology. This $490 (100) dot-matrix display has a removable fluorescent-tube backlight assembly and a built-in backlight voltage inverter and contrast controller. The EG-9002 is available in three versions: a supertwist display with blue characters on a white background; a supertwist display with white characters on a blue background; and a film-supertwist display with black characters on a white background. The EG-9002 is available as a reflective display ($400) or as a backlit display ($450 (100)).

Optrex Corp makes a wide range of dot-matrix modules, including several large-area supertwist displays. Its DMF6106, for example, has an 8.6×6.5-in. (10.7-in. diagonal) viewing area. Priced at $350 (1000), this display features a resolution of 640×480 pixels and a dot pitch of 0.33×0.33 mm. Optrex is also developing color displays with 6-, 9-, and 11-in. diagonal measurements, which it expects to introduce to OEM customers by the middle of 1990 at prices in the $500-to-$600 range.

Although large, high-resolution displays may represent the state of the art and are undoubtedly the most

> The ultimate LCD may be the active-matrix, thin-film-transistor display, which has a contrast ratio of 40:1 and a viewing angle greater than ±45°.

interesting LCDs, smaller displays, including segmented and dot-matrix types, account for the largest share of the market. These types of displays find application in such diverse products as gasoline pumps, medical instruments, test equipment, printers, typewriters, automotive-dashboard displays, industrial controls, and even games and toys.

Typical of many of the industry-standard, dot-matrix LCD modules is a family of devices from Philips Components. The LTN221R/F-10, LTN222R/F-10, and LTN242R/F-10 display two rows of 20, 24, and 40 characters, respectively. The displays have a 5×7-dot character size plus a cursor. Each type is available in reflective (R) and transflective (F) versions; the transflective versions are available with optional green backlighting. All of the modules include a microcontroller with a 160-character ROM and an 8-character RAM for user-definable symbols. The controller accepts 4- or 8-bit parallel data and features an extensive instruction set. Each module comes on a single pc board. The viewing

Manufacturers of LCDs

For more information on LCDs such as those described in this article, circle the appropriate numbers on the Information Retrieval Service card or use EDN's Express Request service. When you contact any of the following manufacturers directly, please let them know you saw their products in EDN.

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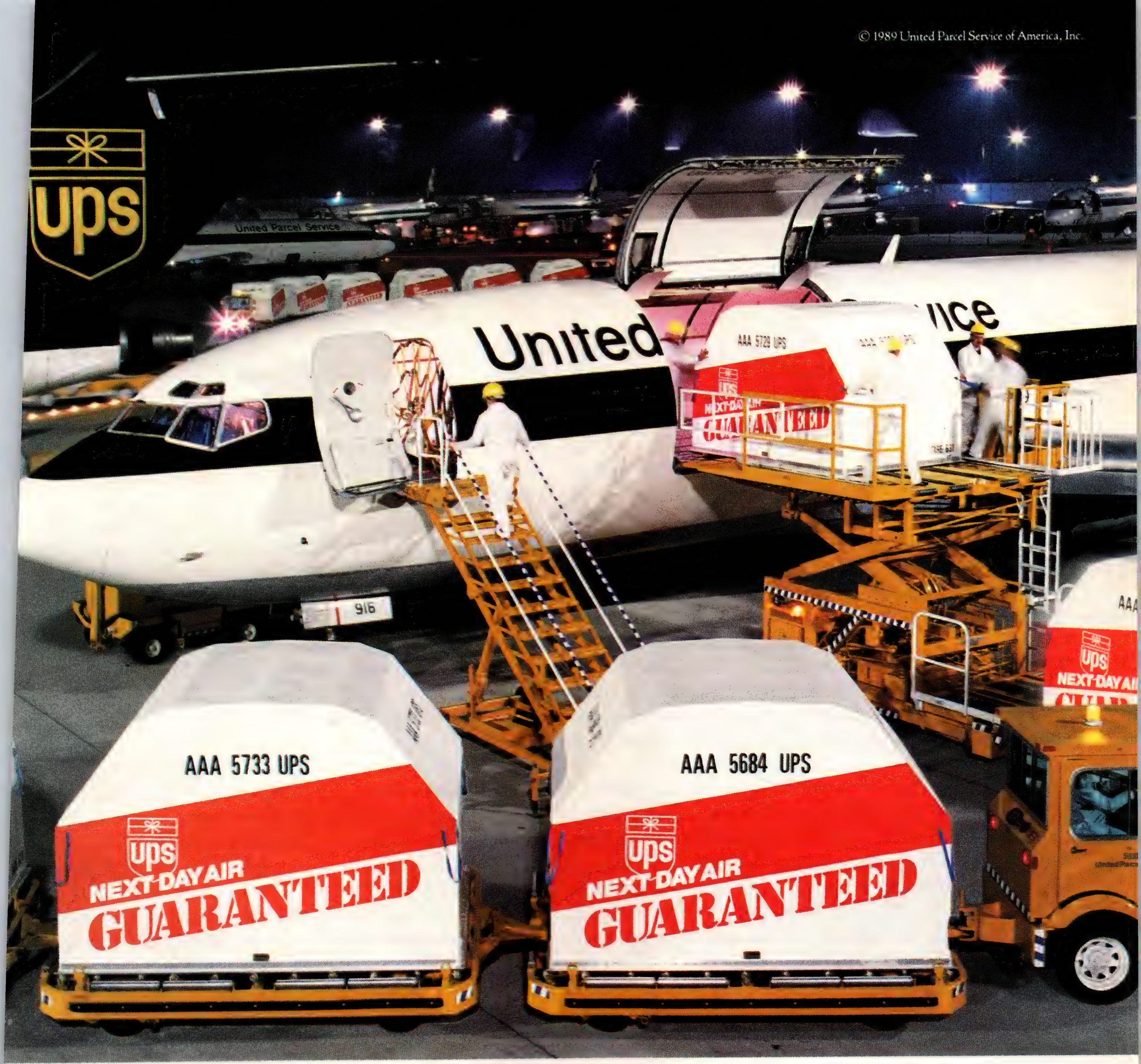

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Most high-performance LCDs require an electroluminescent or fluorescent backlight for optimum performance.

area is 3.2×0.73 in. for the LTN221 and LTN222 and 6.07×0.62 in. for the LTN242. Prices range from Hfl 28 to Hfl 50 (1000) in Holland. Prices vary depending on the importing country.

In addition to a range of character displays, AND offers dot-matrix displays that are suitable for graphics. Its AND1301VST has both driver and controller ICs built into the module. The supertwist, 240×128-dot LCD can simultaneously display graphics and text information. The controller, display RAM, character-generator ROM, and display drivers—all of which are integrated into the module—provide a direct interface to a CPU. The display's viewing area is 7×4 in., and the pixel size is 0.66×0.66 mm. In its standard configuration, the AND1301VST is a reflective display, but fiber-optic and electroluminescent backlights are available as an option. The base price of the display is $227.45 (100).

Although it primarily manufactures customized displays for OEM applications with annual quantities of 10,000 pieces or more, Citizen America Corp also offers several standard displays. These displays have 2.5- to 5.0-in. diagonals and are typically medium-resolution types. The UB-401 (black-and-white) and UC-401 (color) displays, for example, have 4-in. screens with resolutions of 640×110 pixels. The displays, which interface with standard NTSC and RGB signals, are less than 16 mm thick and come with a fluorescent backlight. In 100-piece quantities, the displays cost $217 and $244, respectively.

In addition to the companies already mentioned, there are many others that supply various types of LCDs. Space does not permit a discussion of their products, but you will want to look into the offerings of manufacturers such as Densitron, Hantronix, IEE, LXD, Panasonic, SAI Technology, and Rohm. Densitron, for example, makes dot-matrix alphanumeric displays as well as large graphics displays with resolutions as great as 640×480 pixels. IEE is a well-known supplier of many types of flat-panel displays, including a wide range of dot-matrix LCDs. LXD and Panasonic make 7-segment character displays, and Panasonic also offers large dot-matrix displays. A newcomer to the US market, Rohm Corp is introducing several supertwist displays with resolutions of 640×200 and 640×400 pixels.

Other companies offer products utilizing liquid-crystal technology that depart from the usual types of displays. Taliq Corp, for example, has its Varilite color displays, which use the company's Nematic Curvilinear Aligned Phase (NCAP) liquid-crystal technology. With these displays, it is possible to position a display window on top of a membrane switch pad. When pressed, the touch switch lights up in color, thus providing a visual status indication.

In an even greater departure from the typical LCD panel, Tektronix offers a product that combines a color monitor with a removable liquid-crystal modulator panel. Designed for use in applications such as molecular modeling, crystallography, medical imaging, and defense mapping, the $11,500 SGS-625 offers both monoscopic (2-D) and stereoscopic (3-D) modes. The system features a 19-in. Trinitron color monitor, an easily detachable liquid-crystal stereoscopic modulator, and stereo viewing glasses. The SGS-625 has a resolution of 1280 pixels×1024 lines at a 60-Hz frame rate; the resolution changes to 1280 pixels×512 lines at a 120-Hz frame rate. The large-area, screen-sized modulator provides different polarization for the left- and right-eye images, as seen through the viewing glasses.

At the risk of reciting the obvious, it is clear that there's an LCD for nearly every application. Moreover, new product developments are rapidly filling existing gaps. As product enhancements continue and manufacturing costs decline, you can expect to see LCDs used in continually increasing numbers in even more applications. EDN

Reference

1. Silverstein, Melvin F, "How To Select a Flat Panel Display," *1989 Designer's Guide Series*, Beta Review Inc, Medfield, MA.

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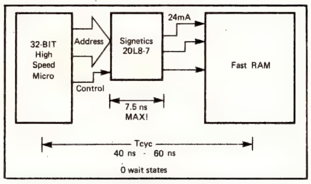

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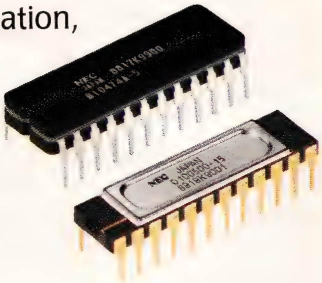

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B10470D-10/-15		4K x 1	10/15			18-pin ceramic DIP
B10474AD-5/-6		1K x 4	5/6			24-pin ceramic DIP
B10474D-8/-10/-15			8/10/15			24-pin ceramic DIP
B10480D-10/-15		16K x 1	10/15			20-pin ceramic DIP
B10480B-10/-15						20-pin ceramic flat
B10484D-10/-15		4K x 4	10/15			28-pin ceramic DIP
B10484B-10/-15						28-pin ceramic flat
D10500D-15/-18		256K x 1	15/18			24-pin ceramic DIP
B100422D-7/-10	ECL 100K	256 x 4	7/10	1.0	−4.5±5%	24-pin ceramic DIP
B100422B-7/-10						24-pin ceramic flat
B100470D-10/-15		4K x 1	10/15			18-pin ceramic DIP
B100474AD-5/-6		1K x 4	5/6			24-pin ceramic DIP
B100474AB-5/-6						24-pin ceramic flat
B100474D-8/-10/-15			8/10/15			24-pin ceramic DIP
B100474B-8/-10/-15						24-pin ceramic flat
B100474B-45/-50/-60			4.5/5.0/6.0	2.0		
B100474K-45/-50/-60						24-pin LCC
B100480D-10/-15		16K x 1	10/15	1.0		28-pin ceramic DIP
B100480B-10/-15						28-pin ceramic flat
B100484D-10/-15		4K x 4	10/15			28-pin ceramic DIP
B100484B-10/-15						28-pin ceramic flat
B100484K-10/-15						28-pin LCC
D100500D-15/-18		256K x 1	15/18			24-pin ceramic DIP

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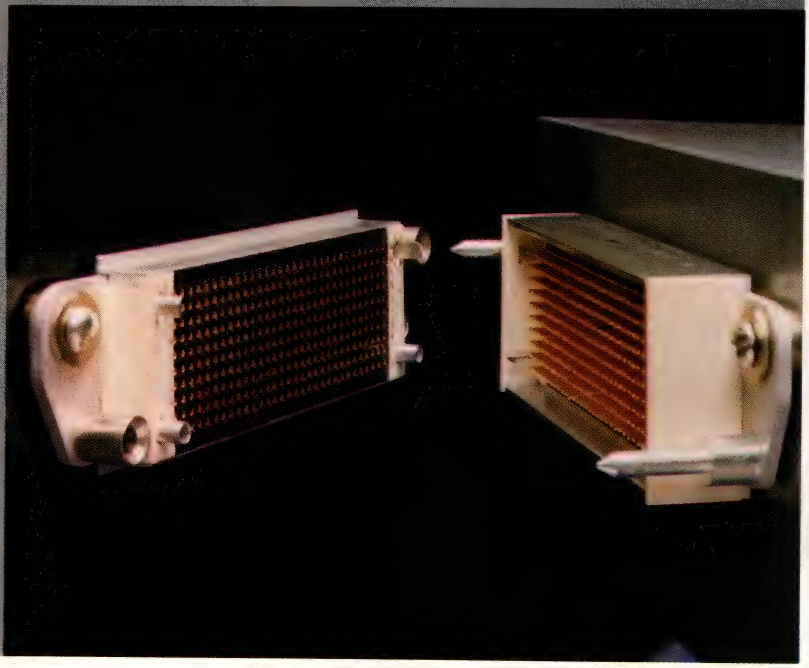

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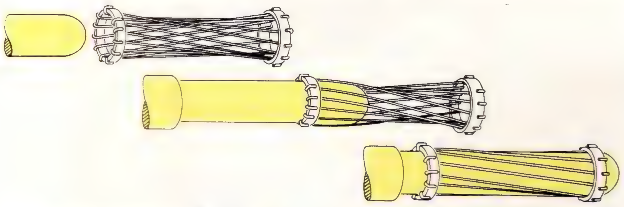

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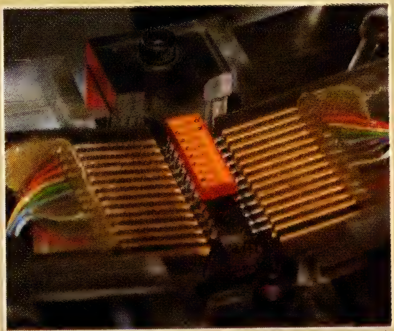

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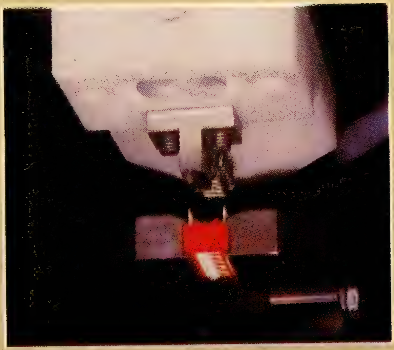

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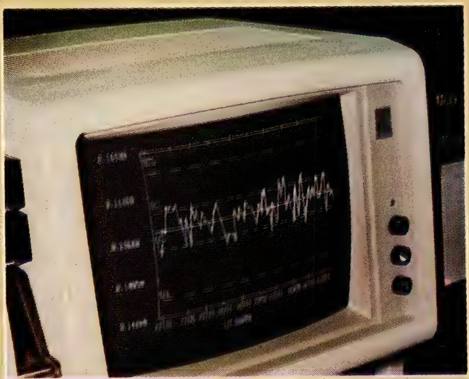

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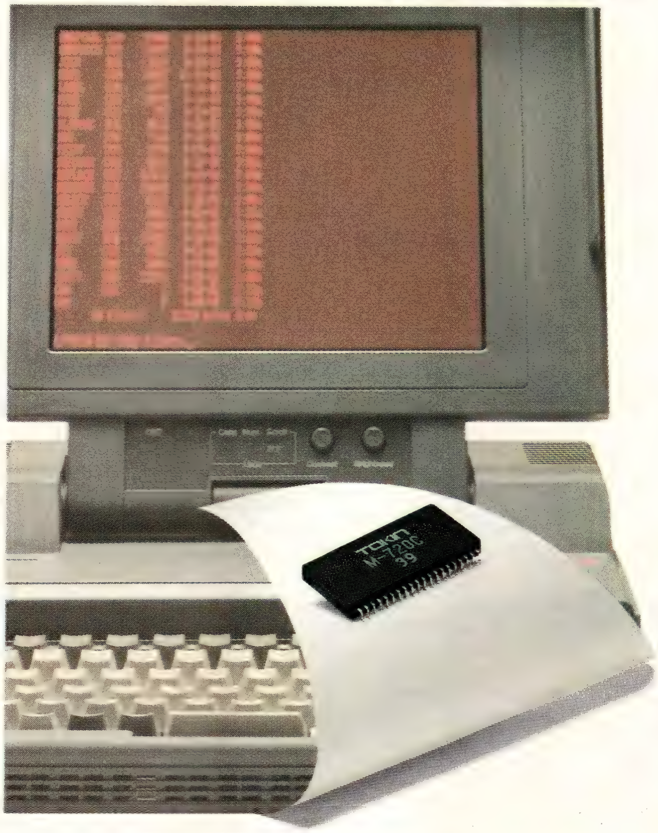

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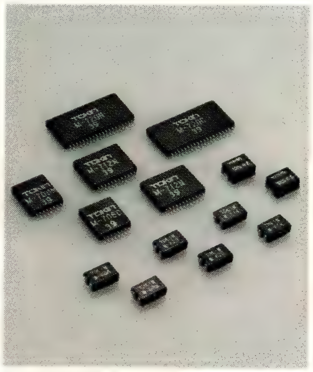

Model	Frequency range (MHz)	Impedance (Ω)	
M-608□	5 ~ 200	≧300 (at 100 MHz)	Common mode
M-614□	5 ~ 100	≧700 (at 50 MHz)	Common mode
M-620□	5 ~ 50	≧1000 (at 300 MHz)	Common mode
M-720N	50 ~ 300	≧100 (at 200 MHz)	Normal mode 20 circuits
M-712N	50 ~ 300	≧100 (at 200 MHz)	Normal mode 12 circuits
M-708N	50 ~ 300	≧100 (at 200 MHz)	Normal mode 8 circuits
M-720C	50 ~ 300	≧70 (at 200 MHz)	Common mode 2 circuits × 10
M-712	50 ~ 300	≧70 (at 200 MHz)	Common mode 2 circuits × 6
M-708C	50 ~ 300	≧70 (at 200 MHz)	Common mode 2 circuits × 4
M-540C	5 ~ 200	≧370 (at 50 MHz)	Common mode 4 circuits
M-580C	5 ~ 200	≧370 (at 50 MHz)	Common mode 4 circuits × 2

S indicates stick types (25 pcs per stick type)
T indicates reel types (1,500 pcs per reel) (16×8 mm pitch, 13″ reel) □ indicates loose types (100 pcs per bag)

Model	Rated current (A)	Inductance Min. (μH)	DC Resistance Max. (mΩ)	Operating temperatue (°C)
SN-S3M-1503□	1.5	3.0	60	−25 ~ +60
SN-S3M-1006□	1.0	6.0	100	−25 ~ +60
SN-S3M-0513□	0.5	13.0	500	−25 ~ +60

T indicates reel types 1,000 pcs per reel (16× 12 mm pitch) □ indicates loose types 100 pcs per bag 13″ reel

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CIRCLE NO 75

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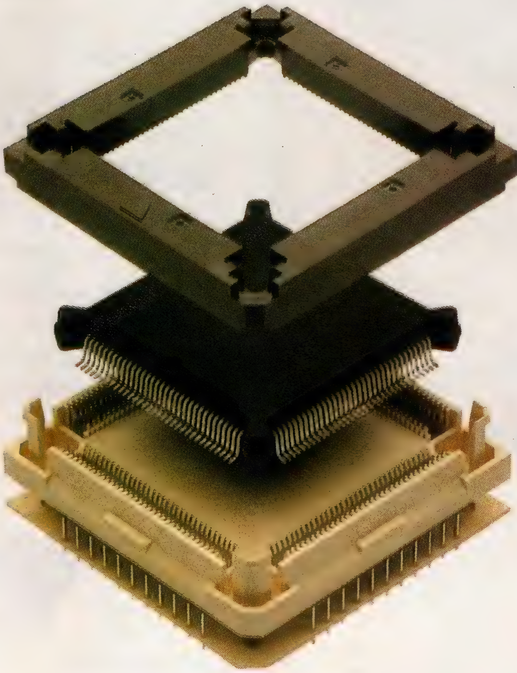

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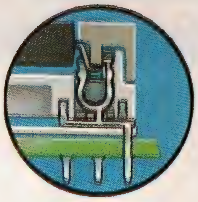

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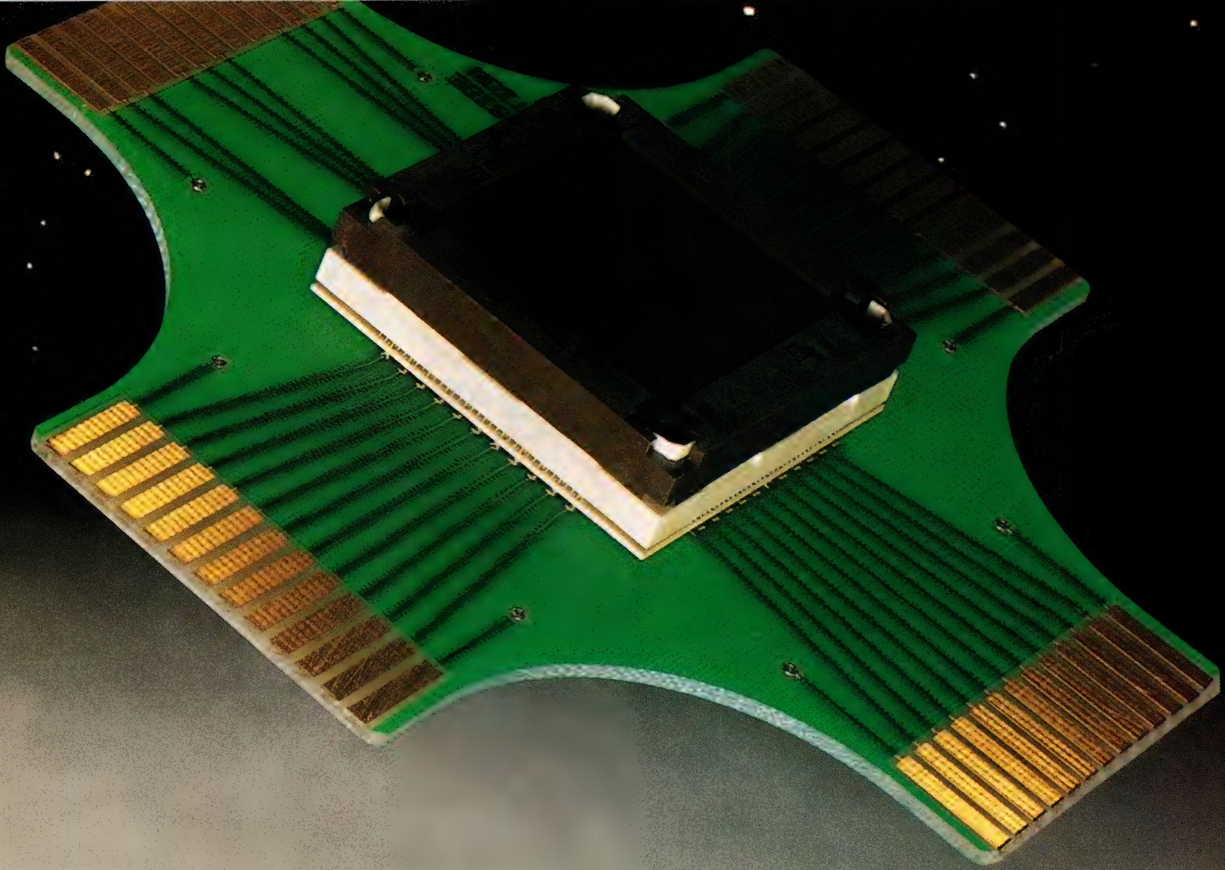

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CIRCLE NO 78

Single-chip DSPs advance in speed and versatility

The insatiable demand for speedy, accurate number-crunching capabilities is fostering the development of DSP chips that exhibit supercomputer-like math performance. Both fixed- and floating-point units are reaping the benefits of intense development efforts.

Bill Travis, *Contributing Editor*

The pressure to process greater amounts of data at faster rates has resulted in awesome computing-power advances, such as million-transistor microprocessors and huge, 4M-bit dynamic RAMs. This desire to process more data even faster is also responsible for comparable progress in the complexity and performance of general-purpose DSP chips. Improvements in older models through die shrinks, process changes, and added "bells and whistles"—as well as the introduction of newer, more powerful DSP ICs—are allowing system designers to keep pace with increasing number-crunching demands.

Table 1, similar to the one in a previous DSP-chip roundup (EDN, October 16, 1986, pg 162), gives a summary of brand-new and yet-to-come general-purpose DSP chips. In that roundup, we outlined the criteria you must consider when choosing a DSP chip. In this directory, you'll find enhanced versions of older devices and several models that didn't exist when we published our last survey. One of the differences between the articles is that this year's table has no "Technology" column, because all new-generation DSP chips are processed in high-resolution CMOS.

As we discuss the products presented in **Table 1**, note that although these devices are general-purpose DSP chips, in many respects they're application-specific; that is, they vary widely in their memory options, bus structures, and number-handling formats. Your choice, of course, depends on the needs of your specific application.

Many of the manufacturers mentioned here have improved their established DSP chips through die shrinks, processing changes, and architectural enhancements. The die shrinks (smaller features) have produced speed increases. One example is Analog Devices' ADSP-2100A, whose multiply/accumulate cycle requires 80 nsec to execute. Its predecessor, the ADSP-2100, required 125 nsec for the same operation. Note that this 56% speed increase exacts a moderate price in power dissipation: 750 mW of full-speed power vs the 2100's 450 mW.

The 2100 family has no onboard program or data RAM, so you'll have to provide some high-speed external memory and an address and data bus to allow access to the memory. The newer ADSP-2101/2102 family incorporates a 2k × 24-bit program RAM and 1k × 16-bit

Text continued on pg 128

TABLE 1—HIGH-PERFORMANCE, GENERAL-PURPOSE DSP CHIPS

MANUFACTURER	MODEL	DATA TYPE	DATA LENGTH (BITS)	MAC INPUT PRECISION (BITS)	MAC OUTPUT PRECISION (BITS)	MAC TIMING (nSEC)	CLOCK RATE (MHz)	INTERNAL RAM (BITS)	INTERNAL ROM (BITS)	EXTERNAL MEMORY (BITS)
ANALOG DEVICES	ADSP-2100A	INTEGER	16	16×16	40	80	12.5	NONE	NONE	PROGRAM 32k×24 DATA 16k×16
	ADSP-2101	INTEGER	16	16×16	40	80	12.5	PROGRAM 2k×24 DATA 1k×16	NONE	PROGRAM 14k×24 DATA 14k×16
	ADSP-2102	INTEGER	16	16×16	40	80	12.5	PROGRAM 2k×24 DATA 1k×16	PROGRAM 2k×24	PROGRAM 14k×24 DATA 14k×16
AT&T	DSP 16A	INTEGER	16	16×16	32	25	40	2k×16	4k×16	64k×16
	DSP32C	FLOATING POINT	24 MANTISSA 8 EXPONENT	32×32	40	80	50	1k×32	2k×32	16M×8 4M×32
FUJITUSU	MB86220	FLOATING POINT	18 MANTISSA 6 EXPONENT	24×24	30	150	40	512×24	2k×30	PROGRAM 64k×30 DATA 128k×30
	MB86224	FLOATING POINT	18 MANTISSA 8 EXPONENT	24×24	30	150	40	512×24	2k×30	128k×24
	MB86232	FLOATING POINT	24 MANTISSA 8 EXPONENT	32×32	32	150	40	512×32	1k×32	PROGRAM 64k×32 DATA 1M×32
MICROCHIP TECHNOLOGY	DSC320C14	INTEGER	16	16×16	32	160	25.6	256×16	4k×16	PROGRAM 4k×16
MOTOROLA	DSP56001	INTEGER	24	24×24	56	74	27	1k×24	544×24	PROGRAM 64k×24 DATA 128k×24
	DSP96002	FLOATING POINT	23 MANTISSA 8 EXPONENT 1 SIGN	32×32	44	74	27	2k×24	1088×32	PROGRAM 4G×32 X DATA 4G×32 Y DATA 4G×32
NEC	µPD77C25 µPD77P25	INTEGER	16	16×16	31	122	8.192	256×16	PROGRAM 2k×24 DATA 1k×16	NONE
	µPD77220 µPD77P220	INTEGER	24	24×24	47	122	16.384	1k×24	PROGRAM 2k×32 DATA 1k×24	PROGRAM 4k×24 DATA 8k×24
	µPD77230 µPD77P230	FLOATING POINT	24 MANTISSA 8 EXPONENT	32×32	55	150	13.333	1k×32	PROGRAM 2k×32 DATA 1k×32	PROGRAM 4k×32 DATA 8k×32
OKI SEMICONDUCTOR	MSM699210	FLOATING POINT	16 MANTISSA 6 EXPONENT	22×22	22	100	40	512×22	PROGRAM 2k×32 DATA 64k×22	PROGRAM 64k×32 DATA 64k×22
	MSM699215	FLOATING POINT	16 MANTISSA 6 EXPONENT	22×22	22	100	40	512×22	PROGRAM 2k×32 DATA 2k×22	PROGRAM 64k×32 DATA 64k×22
SGS-THOMSON	ST18930	INTEGER	16 OR 32	16×16	32	80	20	320×16	PROGRAM 3k×32 DATA 512×16	DATA 4k×16
	ST18931	INTEGER	16 OR 32	16×16	32	80	20	320×16	NONE	PROGRAM 64k×32 DATA 4k×16
	ST18940	INTEGER	16 OR 32	16×16	32	100	20	512×16	PROGRAM 3k×32 DATA 512×16	DATA 64k×16
	ST18941	INTEGER	16 OR 32	16×16	32	100	20	512×16	DATA 128×16	PROGRAM 64k×32 DATA 64k×16
TEXAS INSTRUMENTS	TMS320C25-50	INTEGER	16	16×16	32	80	40	544×16	PROGRAM 4k×16	PROGRAM 64k×16 DATA 64k×16
	TMS320C26	INTEGER	16	16×16	32	100	40	1632×16	PROGRAM OR BOOT 256×16	PROGRAM 64k×16 DATA 64k×16
	TMS320C30	FLOATING POINT	24 MANTISSA 8 EXPONENT	32×32	40	60	33	2k×32	4k×32	16M×32
	TMS320C50	INTEGER	16	16×16	32	50/35	57	8.7k×16	BOOT 2k×16	128k×16
ZORAN	ZR34325	FLOATING POINT	24 MANTISSA 8 EXPONENT	32×32	44	80	25	128×32	1k×32 COSINE LUT	PROGRAM 16M×32 DATA 16M×32

KEY: MAC=MULTIPLIER/ACCUMULATOR
TBD=TO BE DETERMINED
LUT=LOOK-UP TABLE
PGA=PIN-GRID ARRAY
PLCC=PLASTIC LEADED-CHIP CARRIER
PQFP=PLASTIC QUAD FLATPACK
CLCC=CERAMIC LEADED-CHIP CARRIER
TN=TO NEGOTIATE

ON-CHIP PARALLEL I/O	ON-CHIP SERIAL I/O	EXTERNAL BUSES	LOW-POWER MODE	POWER DISSIPATION (mW)	PACKAGING OPTIONS	AVAILABILITY	PRICE (QTY)	COMMENTS
NO	NO	2 DATA 2 ADDRESS	NO	790	100-PIN PGA 100-LEAD PQFP	NOW	$60 (1000)	SPEED-ENHANCED VERSION OF ADSP2100; USES EXTERNAL PROGRAM AND DATA MEMORY.
NO	YES	1 DATA 1 ADDRESS	YES	825	68-PIN PGA 68-LEAD PLCC	NOW	$54 (1000)	INTERNAL-RAM VERSION OF ADSP2100; ABLE TO LOAD INTERNAL RAM FROM EXTERNAL EPROM.
NO	YES	1 DATA 1 ADDRESS	YES	825	68-PIN PGA 68-LEAD PLCC	NOW	TN	MASK-ROM VERSION OF ADSP2101; PROGRAM RAM PARTIALLY REPLACED BY ROM.
YES	YES	1 DATA 1 ADDRESS	NO	450	84-LEAD PLCC	SAMPLES	$86 (UNITS)	UPGRADED DSP16; OFERS ENHANCED SPEED AND MEMORY. AVAILABLE IN 3.3V VERSION.
YES	YES	1 DATA 1 ADDRESS	NO	TBD	133-PIN PGA	SAMPLES	$145 (UNITS)	UPGRADED DSP32 IN 0.75-μm CMOS. OFFERS ENHANCED MEMORY ADDRESSING AND I/O.
YES	YES	2 DATA 2 ADDRESS	NO	TBD	135-PIN PGA 80-LEAD PQFP	NOW	$25 (1000)	USES ASIC-LIKE DSP CORE WITH SILICON COMPILER FOR SEMICUSTOM DSP DEVELOPMENT.
NO	YES	2 DATA 2 ADDRESS	NO	TBD	80-LEAD PQLC	NOW	$30 (1000)	PROVIDES I^{2}C SERIAL BUS FOR AUDIO AND OTHER SERIAL-INTENSIVE APPLICATIONS.
YES	YES	3 DATA 2 ADDRESS	NO	TBD	208-PIN PGA	NOW	$1000 (1000)	PROCESSES IEEE-754-FORMATTED NUMBERS DIRECTLY IN TWO 75-nSEC MACHINE CYCLES.
YES	YES	1 DATA 1 ADDRESS	NO	600	40-PIN DIP 44-LEAD PLCC 68-LEAD PLCC	SAMPLES	$75 (UNITS)	FULL-FUNCTION MICROCONTROLLER; USES TI'S 320C10 DSP CORE FOR NUMBER-CRUNCHING. TI IS A SECOND SOURCE.
YES	YES	2 DATA 1 ADDRESS	YES	450	88-PIN PGA	SAMPLES	$144 (UNITS)	INCLUDES μ-LAW/A-LAW AND SINE LUTs AND BOOTSTRAP RAM; HAS 3-BUS ARCHITECTURE.
YES	YES	2 DATA 2 ADDRESS	YES	TBD	214-PIN PGA	SAMPLES 4Q89	TBD	PROCESSES IEEE-754-FORMATTED NUMBERS DIRECTLY; COMPATIBLE WITH DSP56001.
YES	YES	1 DATA	NO	250	28-PIN DIP 44-LEAD PLCC	NOW	$12 (10,000)	UPGRADED VERSION OF μPD7720/77C20 SERIES; ENHANCED SPEED, PROGRAM ROM, AND DATA RAM.
YES	YES	1 DATA 1 ADDRESS	NO	1000	68-PIN PGA	NOW	$40 (10,000)	FIXED-POINT VERSION OF μPD77230 FLOATING-POINT UNIT; USABLE IN SLAVE OR MASTER MODE.
YES	YES	1 DATA 1 ADDRESS	NO	1500	68-PIN PGA	NOW	$75 (10,000)	ALL INSTRUCTIONS EXECUTE IN ONE CYCLE; HAS 3-STAGE INSTRUCITON PIPELINE.
YES	NO	1 DATA 1 ADDRESS	YES	400	100-LEAD PQFP 84-LEAD PLCC	NOW	$74.25 (1000)	UPGRADED VERSION OF MSM6992 WITH DOUBLE THE RAM AND ROM; HAS LOWER PIN COUNT.
YES	YES	1 DATA 1 ADDRESS	YES	400	100-LEAD PQFP 84-LEAD PLCC	NOW	TBD	SERIAL-I/O VERSION OF MSM699210.
NO	NO	1 DATA 1 ADDRESS 1 SYSTEM	YES	800	48-PIN DIP 52-LEAD PLCC	NOW	$20 (1000)	HIGHER-SPEED CMOS VERSION OF TS68930.
NO	NO	2 DATA 2 ADDRESS 1 SYSTEM	YES	800	124-PIN PGA	NOW	$60 (1000)	HIGHER-SPEED CMOS VERSION OF TS68931.
NO	YES	1 DATA 1 ADDRESS 1 SYSTEM	YES	800	84-PIN PGA 84-LEAD PLCC	4Q89	$35 (1000)	ENHANCED VERSION OF ST18930; INCLUDES SERIAL CHANNEL FOR CODEC INTERFACE.
NO	YES	2 DATA 2 ADDRESS 1 SYSTEM	YES	800	144-PIN PGA 144-LEAD PQFP	SAMPLES	$70 (1000)	ENHANCED VERSION OF ST18931; INCLUDES SERIAL CHANNEL FOR CODEC INTERFACE.
NO	YES	2 DATA	YES	925	68-PIN PGA 68-LEAD PLCC	NOW	$27 (10,000)	ENHANCED-SPEED VERSION OF TMS320C25.
NO	YES	2 DATA	YES	925	68-LEAD PLCC	SAMPLES	$26 (100,000)	TRIPLES ON-CHIP RAM CAPACITY OF TMS320C25.
YES	YES	2 DATA 2 ADDRESS	NO	1500	180-PIN PGA	NOW	$140 (10,000)	REAL-TIME DSP OPERATING SYSTEM (SPOX).
YES	YES	2 DATA 2 ADDRESS	NO	TBD	84-LEAD CLCC	SAMPLES 1Q90	$500 (UNITS)	INCORPORATES 4-WIRE SERIAL TEST BUS BASED ON JTAG-RECOMMENDED IEEE P1149.1.
NO	NO	1 DATA 1 ADDRESS	NO	1000	84-PIN PGA	SAMPLES	$137 (10,000)	PROCESSES IEEE-754-FORMATTED NUMBERS DIRECTLY; CONTAINS COSINE LUT. HARRIS IS A SECOND SOURCE.

New, more powerful DSP ICs and improvements in older models let you keep up with increasing number-crunching demands.

data RAM. For many applications, the inclusion of this static RAM eliminates the need for fast external-memory chips. It also eliminates the external address and data bus, thereby allowing you to reduce the pin count from 100 to 68.

Other enhancements in the 2101/2102 units include serial ports with autobuffering capability (for automatic transfer of data between each port and the buffers); a programmable interval timer; and programmable wait-state generation. On-chip boot-loading hardware lets you load the internal memory from an inexpensive, 27-Series EPROM. In the 2102, you can choose to replace any program-RAM location by mask-programmable ROM. The code for the 2101/2102 is a superset of the code for the 2100; the newer units are source- and object-code compatible with the 2100. However, you may need to relocate 2100 program code to use the 2101/2102's internal memory.

AT&T's DSP16A 16-bit, integer DSP chips offer markedly higher speeds compared with the company's earlier DSP16 devices. Shrinking feature sizes are responsible for these higher speeds. The new chips, processed in 0.75-μm CMOS technology, are available with 25- and 33-nsec instruction-cycle times vs the older devices' 55 and 75 nsec. As you might expect, you'll have to pay for these increased speeds: in sample quantities, the 25- and 33-nsec parts cost $86 and $68, respectively vs $34.50 and $25 for the 55- and 75-nsec devices.

In addition to increased speed, the DSP16A offers more on-chip memory than the earlier DSP16 units: 4k-word vs 2k-word ROM, and 2k-word vs 0.5k-word RAM. The new, expanded-memory devices maintain source-code, object-code, and pin compatibility with their slower siblings. For battery-powered applications, AT&T offers 3.3V versions of both the DSP16 and the DSP16A. These low-voltage devices provide speeds of 75 and 55 nsec, respectively, and they dissipate only 100 and 125 mW.

Another example of an incrementally improved DSP

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chip is the TMS320C25-50, a 16-bit, fixed-point device from Texas Instruments. This unit, a member of the product family TI dubs "second-generation" DSP circuits, reduces the instruction-cycle time from 100 to 80 nsec, corresponding to an increase in maximum clock rate from 40 to 50 MHz. Object-code and pin compatible with the TMS320C25-50, the recently announced TMS320C26 includes three times the amount of on-chip RAM. As in the case of Analog Devices' ADSP2101/2102 (vs the RAMless 2100 devices), the inclusion of the healthy 1.5k words of RAM saves board space and cuts system costs by eliminating or reducing the requirement for external, high-speed static RAMs. An on-chip boot ROM can configure the on-chip RAM as program memory.

The second-generation TI units just mentioned use CMOS processing rather than the earlier 32020 Series' NMOS. The alluring low power and high speeds of high-resolution CMOS make it the processing method of choice for all new DSP chips, including upgrades of earlier, NMOS-processed devices. Good examples of this process conversion are SGS-Thomson's ST18930/18931 16-bit, fixed-point units. These CMOS versions of the company's TS68930/68931 devices offer both higher speed (80- vs 160-nsec multiply/accumulate timing) and more program ROM (3k vs 1.3k 32-bit words) than the earlier units. The maximum-power rating—800 mW vs 3W—is one of the advantages of the CMOS technology.

New members of SGS-Thomson's CMOS-processed, DSP-chip repertoire are compatible with the ST18930/18931, but they offer expanded features. Model ST18940 and the program-ROMless ST18941 include a serial channel for direct interface with Integrated Services Digital Network (ISDN) ICs, codecs, and other serial-oriented devices. The ST18941's ability to address 64k words of external program memory allows the device to provide true real-time emulation of the ST18940 ROM version. Samples of the two new units will be available at the end of this year.

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CIRCLE NO 77

Many manufacturers have improved their established DSP chips through die shrinks, processing changes, and architectural enhancements.

Perhaps the most ambitious of the NMOS-to-CMOS conversions is AT&T's DSP32C—a 32-bit, floating-point device that uses 0.75-μm CMOS processing. The unit incorporates 405,000 transistors in a 0.136-in.^{2} chip that's housed in a standard 133-pin PGA (pin-grid array). In addition to the process conversion, the company decided to add several features. For example, the doubling of the earlier device's 25-MHz clock rate increases the computation rate from 12.5M to 25M flops.

Expanded memory-addressing and I/O capabilities also grace the DSP32C. The unit's 24-bit address space (vs the DSP32's 16-bit space) allows it to address 16M 8-bit words, 8M 16-bit words, or 4M 32-bit words of external memory. Compare this memory space with the DSP32's 28k×32-bit external-memory capacity. The DSP32C includes a utility to convert (in a single instruction cycle) a single-precision, IEEE-format number to and from the chip's internal floating-point representation. This feature attests to the growing popularity of the IEEE-754 floating-point standard. Further enhancements of the CMOS devices include a 16M-bps (vs 12.5M-bps for the DSP32) serial-I/O port and a 16-bit (vs 8-bit) parallel-I/O port. As usual, you'll have to pay for these enhancements: $117 for the DSP32C vs $47 for the older device.

A recent speed increase in Motorola's DSP56001 24-bit integer processor provides a 30% increase in throughput. The device's 27-MHz operating frequency computes at 13.5 MIPS. This speed, as well as the 24-bit resolution, make the device suitable for such applications as CD-quality sound processing, 2-D graphics, and digital-television functions. The 544-bit internal ROM shown in **Table 1** includes a 256×24-bit, μ-Law/A-Law lookup table; a 256×24-bit, sine-lookup table; and a 32×24-bit bootstrap ROM. The 56001's triple-bus architecture simultaneously handles two pieces of data and an instruction.

New DSP chips

The incessant demand of evolving systems for more processing power at higher speeds has spurred the development of a large number of entirely new chips. Capitalizing on the success of its venerable μPD7720/77C20 family of 16-bit, fixed-point devices, NEC has introduced an upgraded version called the μPD77C25. (An EPROM version, the μPD77P25, is also available.) The new units are pin compatible with the 7720 devices, and they execute instructions twice as fast (122 vs 250 nsec). Additional enhancements include four times the program-ROM space (2k vs 0.5k words) and twice the data-RAM capacity (256 vs 128 words).

NEC's μPD77220, a fixed-point version of its μPD77230 floating-point processor, processes 24-bit data in 122 nsec. Except for floating-point operations, the new, pin-compatible device is software compatible with the μPD77230. You can use the device in either master or slave mode. In master mode, you can add 8k words of external memory, of which you can use 4k words as an instruction area. In slave mode, the device operates as an I/O processor for the host CPU.

Texas Instruments has expanded its extremely successful 320 family of DSP chips with the TMS320C30, a chip introduced last year, and a couple of devices that are on the way. The TMS320C30 is a 32-bit, floating-point unit that incorporates 695,000 transistors and features a 60-nsec multiply/accumulate time. The million-transistor Model TMS320C50, a fixed-point device slated for sampling in the first quarter of next year, will incorporate four times more RAM (8.7k words) than any other chip on the market. The device will execute a 16-bit, integer multiply/accumulate function in 35 nsec (after production ramp-up—first samples will execute in 50 nsec).

The TMS320C50 will be the first DSP chip to incorporate the industry-standard, 4-wire serial test bus based on the recommendations of the Joint Test Action Group (JTAG) and defined by IEEE P1149.1. The bus, based on boundary-scan techniques, lets you use the device as a self-emulator; it also allows board-level testing via the 4-wire interface, as opposed to the traditional bed-of-nails approach. The enhanced instruction set of the TMS320C50 is source-code compatible with previous generations of TMS320C10 and TMS320C20 devices. Later this year, TI will reveal details about its TMS320C40 Series of third-generation, floating-point DSP chips.

Many system designers require the speed and power of DSP number crunching in addition to general-purpose computing. To satisfy this need, Microchip Technology Inc, in collaboration with TI, has developed a microcontroller that uses TI's 320C10 DSP unit as a core. The 16-bit, fixed-point DSC320C14 has a 160-nsec instruction cycle. Therefore, its math speed is five to ten times that of conventional microcontrollers.

An apt application for a combined microprocessor/DSP unit is in closed-loop control systems, which generally use second-order FIR and IIR filters in the feedback loop. The number-crunching demands of these digital filters often make it impossible to achieve real-

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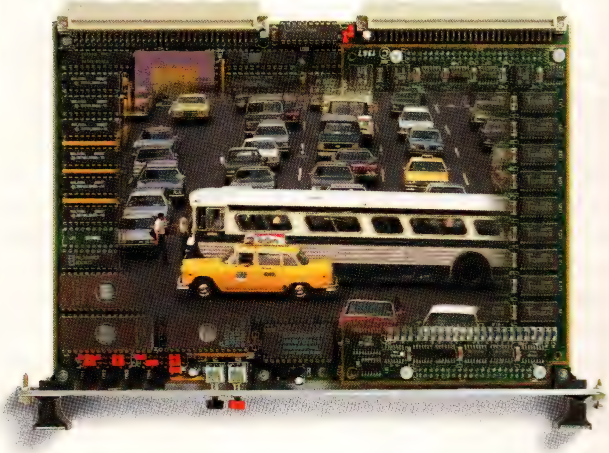
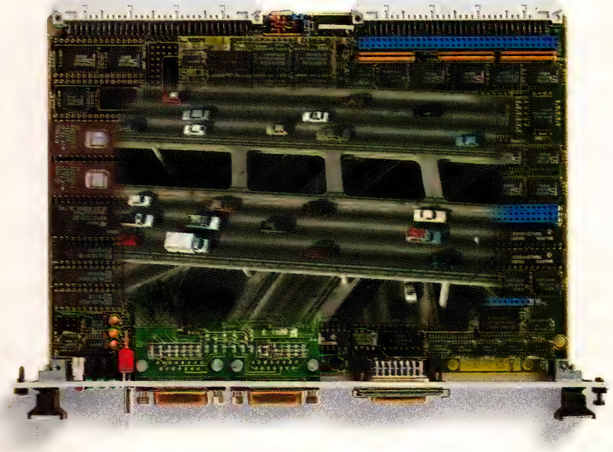


Arbitration Delays



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CIRCLE NO 79

The alluring low power and high speeds of high-resolution CMOS make it the processing method of choice for all new DSP chips.

time control using available 16-bit microcontrollers.

As if to underscore its applicability to industrial-control systems, the DSC320C14 incorporates 16 software-configurable, latched I/O lines. These lines are user-configurable as either input or output, and you can use them, for example, to directly control such on/off actuators as valves or relays. You can group the input-configured lines so that the IC generates an interrupt when the aggregate value of the lines matches a preset value stored in an I/O buffer register.

Some applications need a higher dynamic range than fixed-point DSP chips can provide. Floating-point devices are able to process an enormous span of numbers without losing accuracy or overflowing, so you can use them for such demanding applications as 3-D graphics, advanced robotics, and speech analysis. Some new floating-point chips from Oki, Fujitsu, and Zoran, as well as a soon-to-be-sampled unit from Motorola, provide the dynamic range these applications require.

Two recent devices from Oki Semiconductor represent an upgrade of the company's MSM6992 22-bit, floating-point unit. The MSM699210 has the same architecture as the earlier MSM6992, but it doubles the internal RAM space to 512 words, and it also doubles the internal ROM to 4k words. In addition, it cuts the pin count from 132 to 100 (84 in a PLCC) by using one bus for both the external data and program buses. The device accommodates 22-bit (16-bit mantissa, 6-bit exponent, or 22E6) floating-point data and 16-bit integer data. The MSM699215 is identical to the MSM699210, except that it offers the advantage of a serial-I/O bus.

New chips from Fujitsu Microelectronics squarely address the need for floating-point math capabilities. The 24-bit (18-bit mantissa, 6-bit exponent, or 18E6) MB86220 is unique in that it offers a semicustom approach to DSP-chip design. By using Fujitsu's silicon compiler, you can configure its ASIC-like DSP core for various I/O configurations, data lengths, and hardware protocols. For audio applications, for instance, you might want to configure a Philips-type I^{2}C serial bus protocol. In fact, a variation of the MB86220—the MB86224—addresses audio applications by providing the I^{2}C protocol.

Perhaps the most significant development in 32-bit, floating-point DSP devices is the direct, 1-cycle processing of numbers in the IEEE-754 format. To achieve IEEE compatibility, most 32-bit chips require a conversion that can take from one to 21 extra cycles to effect. Fujitsu's new MB86232 is the first available chip that performs the IEEE formatting directly. In addition to its 32-bit (24E8), floating-point capability, it handles fixed-point and integer operations. The de-

For more information . . .

For more information on the general-purpose DSP chips discussed in this directory, circle the appropriate numbers on the Information Retrieval Service card or use EDN's Express Request service. When you contact any of the following manufacturers directly, please let them know you saw their products in EDN.

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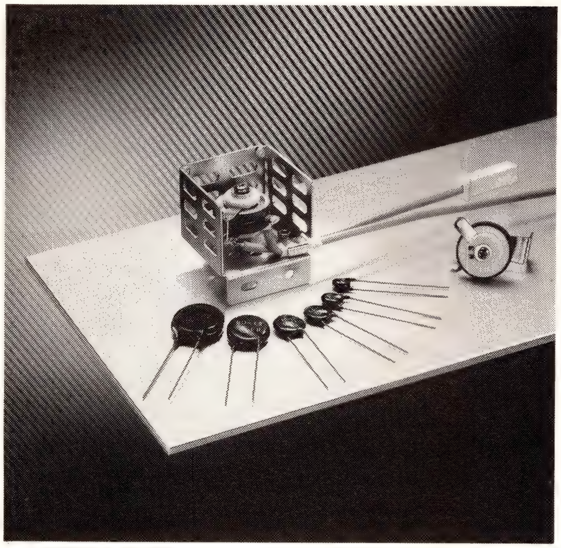

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CIRCLE NO 81

vice requires two 75-nsec cycles to effect a 32-bit, floating-point, multiply/accumulate operation.

Another chip, currently available in sample quantities, processes IEEE-754 numbers directly. Model ZR34325 from Zoran Corp executes a 32-bit, floating-point multiply/accumulate in 80 nsec. Harris Semiconductor will be a second source for the device. The ZR34325 contains 128 words of RAM and no program ROM (with the exception of a 1k×24-word cosine-lookup table). The chip can address 16M 32-bit words each of external program and data memory. The already fast device, currently fabricated in 2-μm CMOS technology, will enjoy a reduction in feature sizes to submicron levels, resulting in significantly higher speeds.

Motorola's DSP96002, a product that's received a lot of advance publicity in the trade press, will be available in sample quantities at the end of this year. The chip can perform IEEE-754 floating-point math at a 74-nsec instruction rate. The 96002 is architecturally identical to—and software compatible with—the company's DSP56001 fixed-point unit, and it has two 32-bit address and data buses for extensive addressing capability. Finally, Analog Devices doesn't intend to be left out in the cold with respect to IEEE-754 processing; watch for the announcement of this company's IEEE-compliant, 32-bit, floating-point device.

In the future, you can expect to see speedier, more powerful, and more versatile DSP chips. For example, chip manufacturers are working on devices that incorporate an analog front end—A/D-converter inputs that accept analog signals directly, convert them to digital form, then perform DSP functions such as digital filtering and fast Fourier transforms.

Finally, DSP-chip manufacturers aren't concerned solely with what goes on the silicon wafers. They're expending considerable effort on the software tools that accompany the chips. Efficient C compilers, as well as simulators, linkers, and other development tools, are available for all the advanced chips. In addition, several third-party vendors have developed high-level-language packages that eliminate the need for complex and esoteric assembly-language (or even C) programming. EDN

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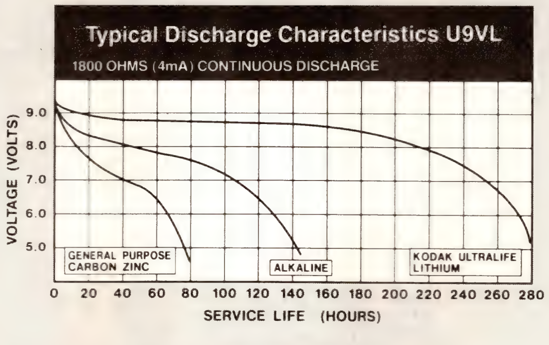

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Make your surface-mount pc boards testable

To achieve higher performance in less space, designers are using surface-mount devices on pc boards that comprise state-of-the-art electronic systems. However, even the most technically elegant and sophisticated surface-mount design is useless—unless you can also test and manufacture it profitably.

Katherine Gambino and John Kenney III,
Valid Logic Systems

Testing and manufacturing issues, primarily related to accessing test points and soldering devices onto the substrate, limited the early adoption of surface-mount technology (SMT). In spite of advances in manufacturing technology that have overcome many of the adhesion problems, progress in SMT testability continues to lag. One reason is that little attention is given at the design stage to solving the test problems associated with surface-mount boards.

Surface-mount designs present you with a different set of testing and manufacturing challenges than traditional through-hole projects. For boards that you design using through-hole components, testability is relatively easy to guarantee. All pins are accessible from the solder or bottom side, making it possible to use traditional bed-of-nails fixturing. In addition, most through-hole component pins are designed with 100-mil pitch spacing to perfectly align with the 100-mil gridding system of most test fixtures.

Guaranteeing test access for an SMT board is quite another story. The characteristics that make surface-mount components so desirable—decreasing space and increasing capability—are directly opposed to the mandates of testability. Surface-mount parts can have 50-mil, 40-mil, or even narrower spacing. Pad sizes are 50×25 mil or smaller, creating conditions that are impossible for traditional board-test fixtures to handle.

Unfortunately, scaling down the test-fixture instrumentation isn't the answer. Test probes of 50 mils or smaller are extremely fragile and much more expensive than their thicker, 100-mil, through-hole testing counterparts. Furthermore, because SMT pads rest only on the two surface layers, many of the pins are inaccessible from the other side of the board. Therefore, without careful design of the SMT board to prepare it for traditional testing techniques, you can't use conventional bed-of-nails, from-the-bottom-up testing methods, where the tester pins make contact from the solder side of the board at either through-hole pad sites or at through-hole vias.

Some companies have tried to retain their conventional automatic test equipment (ATE) while modifying the fixturing technique. For example, clamshell fixtures make access to the surface-mount test points possible from both the top and bottom simultaneously. But, especially in high-speed applications, the resulting hard-wire connections from the top-side fixture to the

Tight pitch spacings and small pad sizes required by SMT boards almost render traditional board-test fixtures obsolete.

test instrument can be much longer than from the bottom-side fixture, resulting in potentially erroneous test data (**Fig 1**). In addition, developing a clamshell fixture is two to three times more costly than a bed-of-nails fixture. This expense is a result of the clamshell fixture being hinged at one end, the difficulty involved with both aligning the probes to the test sites and ensuring the probes' clearance around the components, and the frailty of the probes themselves.

Even if you were to probe on the SMT-component side of the board, another problem arises. Assume that one of the SMT pads isn't adequately adhering to the surface, and the pad has begun to curl up or "lift." The downward force exerted on the pad by the test probe may be sufficient to push the pad back into place and make the connection during the test loop, showing a successful test operation. However, when the probes are removed after the test, the SMT pad will lift again, which could cause the board to fail during actual use. To minimize this risk, don't test SMT-component pins directly. Instead, create test points adjacent to the desired pin. Allow for test-pad accessibility from whatever side of the board the test fixture is designed—bottom, top, or both.

The best way to locate the test point is to remember that surface-mount boards usually have components mounted on both the top and bottom. In addition to placing the test point adjacent to the desired pin, you should also be careful not to create the test pad under a component on the opposite side of the board, since the probe will not be able to access it.

One viable but unattractive option you can use to guarantee accessibility is to provide a test point, in the form of a through-hole via, for every surface-mount pin. This method may improve testability, but it complicates routing the board. SMT boards, by their very nature, are much more dense than through-hole designs. Typical SMT densities range from 0.12 in.^{2} per IC to 0.40 in.^{2} per IC. If you create through-hole test pads for every pin, the very benefits of SMT are lost, since vias consume valuable board real estate on every layer.

Physical placement of test points is only one concern in designing pc boards for testing and manufacturing. You also need to consider the selection requirements for the test points. If the test engineer uses the schematic for determining the required test points, unforeseen problems can occur later in the product cycle. For example, if you don't record all spare parts or gates on the schematic and you later write an engineering change order (ECO) that uses a spare part, the test engineer will have to modify the test fixture to provide access to the new part. Since the pc-board layout is where you do the physical packaging, a more

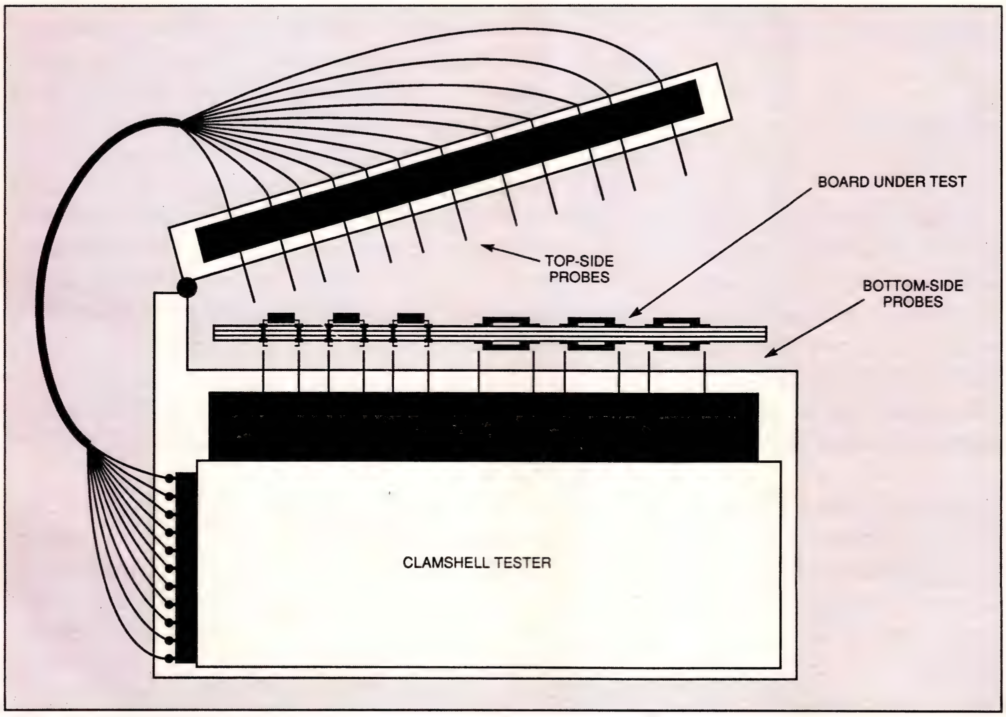


Fig 1—Clamshell fixtures provide simultaneous test access from the top and bottom sides. *However, because the top-side wire connections are longer than the bottom-side connections, they can provide erroneous data in high-speed test applications.*

accurate phase at which to determine test-point criteria may be at the initial physical-design stage. And if you're using a CAD system to implement the surface-mount layout, you should be able to use a test-point selection and access routine in the software, similar to the tools available today for automatic routing and placement.

Designing for accessibility means providing a test point on the pc board that has the correct size, spacing, and positioning to accommodate some form of probing. Also, component packaging must not obstruct the test point. And, to provide complete observation for testing with an ATE system, all nets should be physically accessible using the least costly fixturing technique—the bed-of-nails approach. Whether you manually or automatically (with the assistance of a CAD system) provide test points, the testability requirements are identical. A CAD-based approach, however, will be orders of magnitude faster, and theoretically, more comprehensive and accurate.

Ideally, the CAD-based automatic selection of test points should provide some user-definable criteria for determining the types of pins and the most appropriate point on the net to access. For example, a set of rules or parameters which allows you to instruct the software to select all output pins as test points virtually assures access to all existing and potential nets.

Assign test points with an eye toward ECOs

If you manually assign the test points by using either random selection or simplistic criteria, like the first pin on every net, future ECOs may cause test problems. Consider a potential change like that in **Fig 2a. Figs 2b** and **Fig 2c** illustrate that when you randomly select the first pin on a net as the access point, the change resulting from an ECO would allow a portion of the net to remain untested.

An automatic solution that uses all component outputs as access points **(Fig 2d)** ensures the net's current and future testability. The minimal expense of including these extra test points is dwarfed by the cost of reworking your test fixture should testability requirements and an ECO make it necessary. You can also select the test points by using other criteria, such as 3-state pins and input pins.

CAD-based, automatic-test-preparation software should also let you use other requirements such as grid location, test-point size, test-pad type, and top or bottom access to choose your test points. For example, if you direct the software to only select vias or

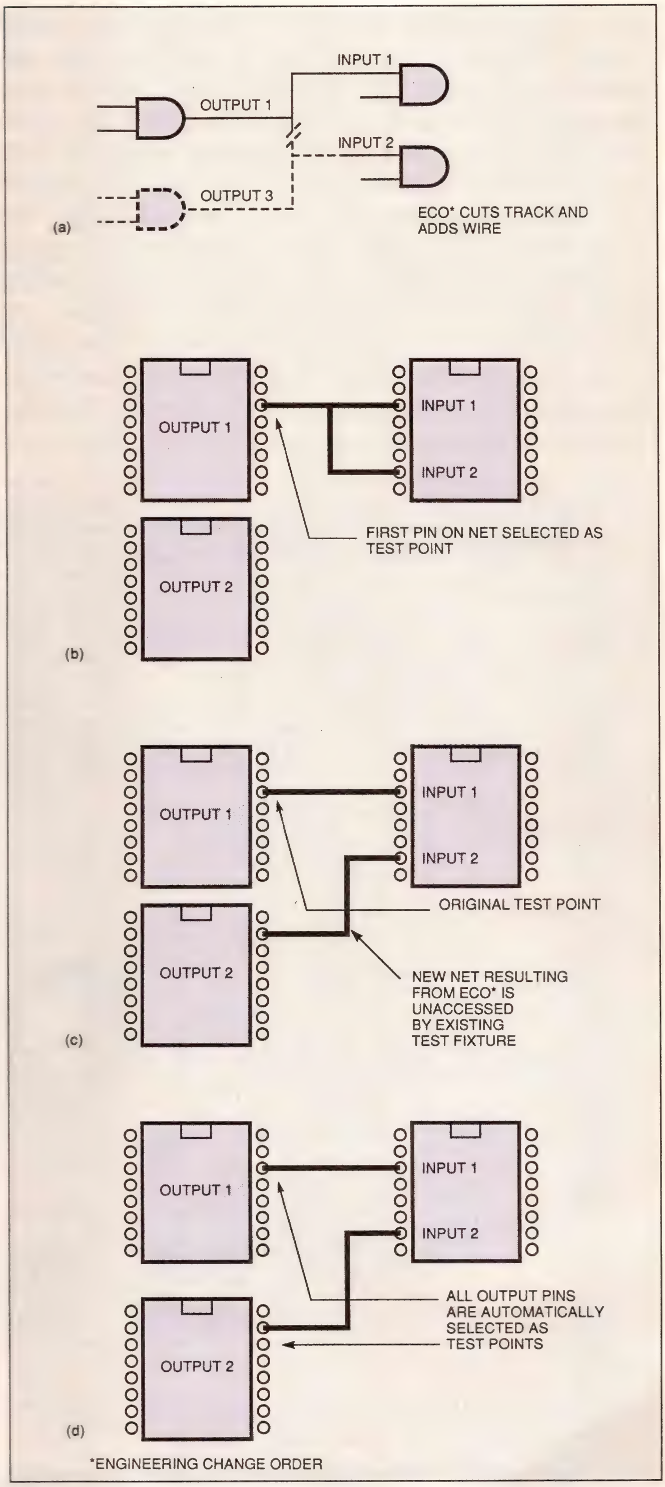

INPUT 1
OUTPUT 1
INPUT 2
OUTPUT 3
(a)
ECO* CUTS TRACK AND ADDS WIRE
OUTPUT 1
INPUT 1
INPUT 2
FIRST PIN ON NET SELECTED AS TEST POINT
OUTPUT 2
(b)
OUTPUT 1
INPUT 1
INPUT 2
ORIGINAL TEST POINT
OUTPUT 2
NEW NET RESULTING FROM ECO* IS UNACCESSED BY EXISTING TEST FIXTURE
(c)
OUTPUT 1
INPUT 1
INPUT 2
ALL OUTPUT PINS ARE AUTOMATICALLY SELECTED AS TEST POINTS
OUTPUT 2
(d)
*ENGINEERING CHANGE ORDER

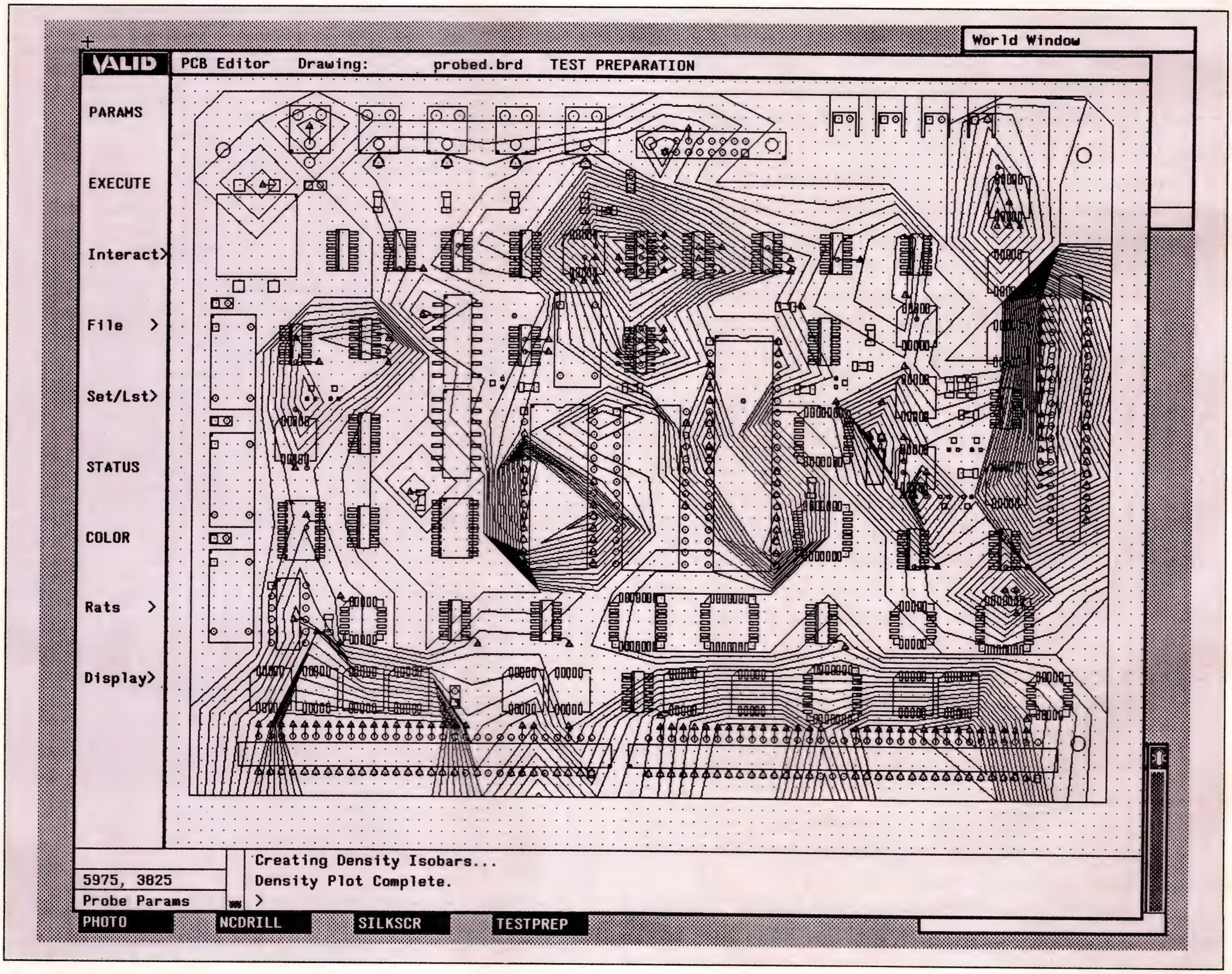
Fig 2—Making a simple change to your circuit *can seriously impact testability* ***(a)****. If you use the first pin on the net as the test point* ***(b)****, the new net won't be testable* ***(c)****, whereas using all the output pins as test points ensures testability* ***(d)****.*

If you probe from the component side of an SMT board, you may mask problems caused by SMT pads lifting off the board.

generate test points that fall on a 100-mil grid, you'll lower the fixture-tooling cost. A test-point-size parameter can ensure that the selected test point is large enough for probing. If the pad is too small, the probe may bend slightly and slip off the pad. When the software generates the test points, they consist of flagged vias, whose size, shape, and levels you can define. You designate multiple types of vias so that, if you are going to perform single-side testing, the software can add a single-layer test point. Such capability minimizes the use of through-hole vias, thus preserving more board space. Finally, a parameter that prevents the software from selecting or generating test points under the component bodies is invaluable in preventing the access points from being unreachable.

Once the software has selected test points on those nets that meet the selection criteria, the software can then create test points for those nets that don't. These CAD-generated test points are put in as vias so that an automatic router can properly connect them. However, for surface-mount devices (SMDs) that are on the same side as the tester-pin probes, the software inserts test pads of user-specified size rather than vias that would clog routing channels on all the other board layers. To avoid excessively long wire delays, you can control the via's or test pad's displacement from the target pin.

Because the software generates all the test points



5975, 3825
Probe Params

Creating Density Isobars...
Density Plot Complete.
>

Fig 3—Software can generate density plots, *which graphically illustrate the distribution of test points. Congested areas are often very difficult to create test fixtures for.*

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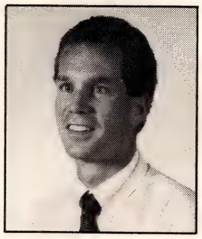
within the CAD database, you should also be able to generate the numerically controlled (NC) drilling data to create the test-fixture probe plate. You can also extract documentation containing drill drawings, probe-hole numbers, and pin and net assignments from the same database.

An electromechanical problem associated with the proper design of an SMD board for testing is the distribution of the test probes. When you place the board into the vacuum-actuated fixture, there must be a relatively even distribution of test probes across the design. Too many probe points in one area can cause the vacuum seal to fail or the board to bend, resulting in loss of contact with the probes and an unsuccessful test process. If you can also visually check for these conditions using graphical density mapping aids, as in **Fig 3**, you can make interactive adjustments to the automatic selections of test points to distribute the points more evenly.

CAD-based approaches to test preparation are becoming popular, and a few vendors offer some or all of these capabilities. Nonetheless, whether you use manual or CAD-assisted design techniques, up-front attention to testing and manufacturing in the layout of your SMT boards will improve the chances for a speedy and accurate cycle through testing and production. **EDN**

Authors' biographies

Katherine Gambino is the director of pc-board product marketing for Valid Logic Systems. She is a 5-year veteran of Valid and has a BA from Barnard College, Columbia University (New York, NY). Katherine directs Valid's marketing activities related to pc-board design and -analysis software.



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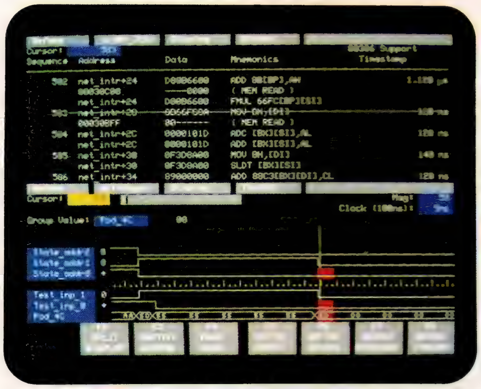

```
Cursor:                                                  80386 Support
Sequence  Address       Data        Mnemonics              Timestamp
   582   net_intr+24   D0006600   ADD 80[BP],AH             1.120 µs
         00030C00      ------0000 ( MEM READ )
         net_intr+24   D0006600   FMUL 66FC[BP][SI]
   583   net_intr+20   0066F00A   MOV DH,[DI]                 100 ns
         000308FF      00------   ( MEM READ )
   584   net_intr+2C   0000101D   ADC [BX][SI],AL             120 ns
         net_intr+2C   0000101D   ADD [BX][SI],AL
   585   net_intr+30   0F3D0A00   MOV BH,[DI]                 140 ns
         net_intr+30   0F3D0A00   SLDT [BX][SI]
   586   net_intr+34   89000000   ADD 88C3[BX][DI],CL         120 ns
Cursor:                                                   Mag:
                                                 Clock (100ns):
Group Value: Pod_4C      00
```

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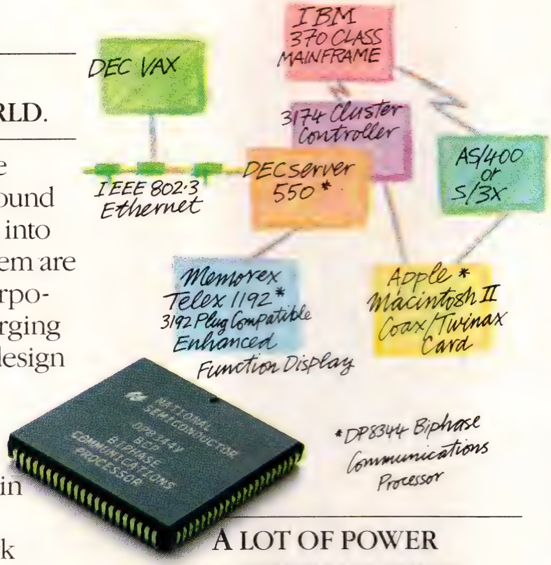
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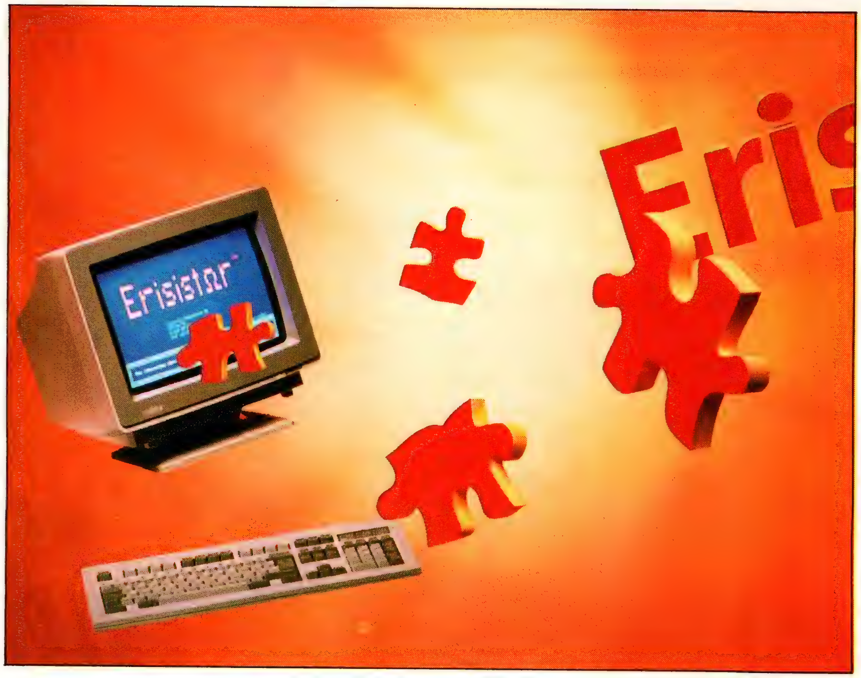

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CIRCLE NO 88

DESIGNER'S GUIDE

microcontroller
simulation
Part 2

Simulation helps you debug I/O software for embedded systems

Part 1 of this 2-part article discussed key issues in design-verification testing and presented a simple example of how a simulator can help you test for potential hardware failures. Part 2 presents another, more complex, example of the use of simulation to debug difficult real-time problems.

Anders Gezelius, *Archimedes Software Inc*

It is not unusual for a system that handles various individual events properly to fail when multiple events occur simultaneously. If some of these events occur infrequently in normal operation, these worst-case combinations may not occur during normal testing.

For instance, the control program for the μC in a full-feature telephone might properly activate a ringer when an incoming call occurs. It might also dial a string of digits properly when a speed-dialing key is pressed. This same program, however, might fail miserably if an incoming call occurred just as a speed-dialing key was pressed.

Trying to test such a scenario with real hardware can be very difficult. The window in which a failure would occur might be only one instruction time (perhaps 1 μsec) out of the period between event repetitions (perhaps 6 seconds). Testing for this error might require millions of repetitions of the events; thus more than a year could elapse before the fault-producing event sequence would occur. Furthermore, unless you can view the internal operation of the processor, it might be difficult to tell if the desired sequence occurred during the testing period. A simulator, on the other hand, makes it quite easy to generate exactly the sequence you wish to test—and also provides a simple means of viewing the response of the system under test.

To illustrate, let's examine a problem that actually arose in a typical project. We'd been given the task of designing a remote data-acquisition unit that would repeatedly sample the voltage on four analog inputs every 35 msec and transmit the results over a 2000-bps serial link to another system. In addition, the unit would monitor four more analog "alarm" inputs; if the voltage values on one or more of these inputs exceeded a predefined alarm threshold, the unit would transmit the alarm values to the second system.

Fig 1 depicts the hardware configuration. The communications link uses the serial interface built into the 8051; the analog monitoring circuit is an external ADC0808 chip, which contains an 8-bit ADC and an 8-to-1 analog multiplexer.

Fig 2 shows the format for transmitting the serial data. This format calls for the controller to initiate A/D conversions on the four repeating channels (inputs 4, 5, 6, and 7), to store the values, and then to transmit those results in order. After transmitting values for the repeating channels, the controller tests the alarm channels (inputs 0, 1, 2, and 3). If an alarm input has

By accumulating a list of potential trouble spots as your design progresses, you ensure that they all get tested.

changed since it was last reported *and* the new value is above the alarm threshold, the controller sends two bytes. The first byte contains the channel number (0-3) of the alarm input that is being reported; the second is the value sensed on the alarm input.

Because it takes 20 msec to transmit the data for the four repeating channels (5 msec per byte), and 10 msec to transmit an alarm (2 bytes per alarm), this format can transmit only one alarm in each 35-msec sampling period. This restriction is acceptable because the alarm inputs are generated by temperature sensors, which do not change rapidly.

Listing 1 shows a portion of the operational code for the remote data-acquisition unit. It includes the function that reads the ADC, the function that transmits serial data, and the main functional loop.

The main functional loop waits until a 35-msec timer expires, then performs A/D conversions on each of the four repeating channels and transmits the results. Next, the main loop samples each alarm channel and compares the new alarm to the last reported alarm value for that channel in the last<alarm<value array. If the new value is different, it replaces the old value; if the new value is greater than the alarm threshold, the controller sends the new value. As you can see from the code, we handled the restriction of only one alarm per period by not checking any more alarm channels once a qualifying alarm was found. What you can't see is the frustration that set in.

While coding this relatively straightforward algo-

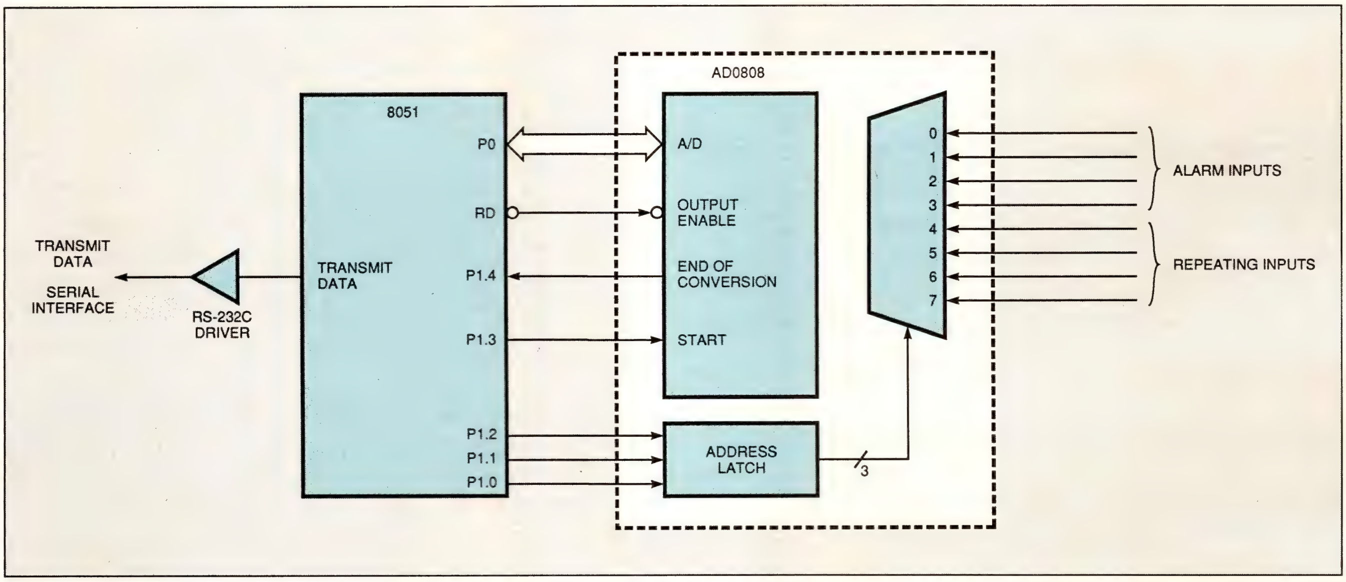

Fig 1—Simulation helped to debug *this data-acquisition unit.*

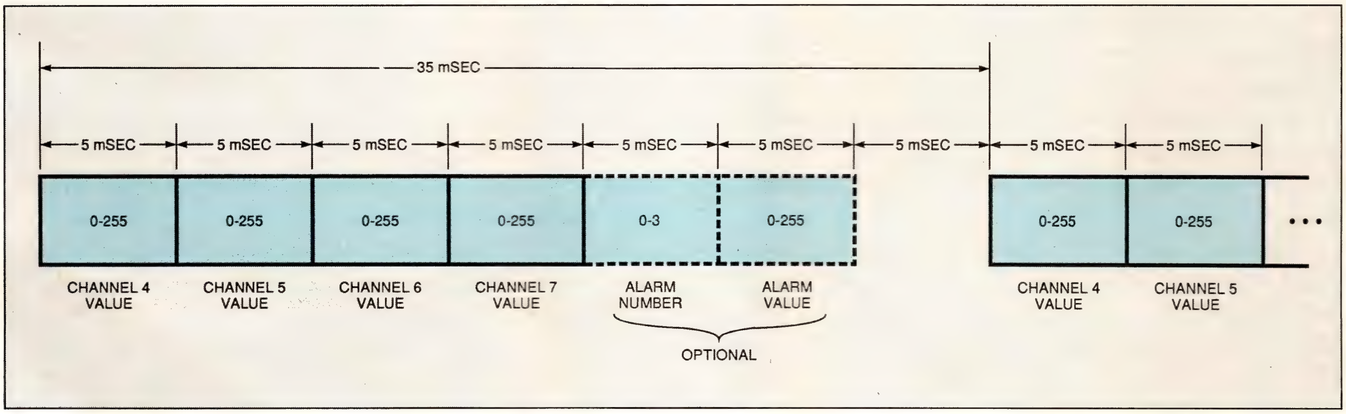

Fig 2—The controller uses this format *to initiate A/D conversions, store the values, and transmit the results.*

rithm for sampling the alarm channels, a troublesome scenario came to mind. It was assumed that if two alarms occurred simultaneously, one of them would be reported during one period and the other would be reported in the next period. This short delay would be acceptable; the inputs were not expected to change rapidly enough that one alarm would keep being reported—thus locking out the other alarm. But what if alarm channel 0 was near the transition between two different alarm values? Couldn't it oscillate back and forth every period so that it would have to be reported each time, and therefore block the reporting of all other alarms?

Effectively, channel 0 was being given highest priority because it was the first one sampled. What was needed was a way to rotate the priority in a round-robin fashion so that each of the different alarm channels would have a turn at highest priority. The solution was quite elegant—only three lines of code had to be changed. The revised alarm-sampling code is given in **Listing 2** (the changed lines are shaded).

This revision used a new variable *(count)* to act as the loop variable and allowed alarm_select to hold its value from one period to the next, rather than resetting it to 0 every time the alarms were tested. This change was supposed to allow the alarm code to begin its checking with the next alarm channel in the sequence, even after an alarm had been reported during the pre-

LISTING 1—OPERATIONAL CODE FOR DATA-ACQUISITION UNIT

```
/*Perform a conversion on the specified channel and return the result*/
unsigned char read_ADC(unsigned char selector)
   {
   output(P1, selector | 0xF0);  /* Output channel select bits */
   set_bit(P1_3_bit);            /* Output ADC START pulse */
   clear_bit(P1_3_bit);
   while (!read_bit(P1_4_bit));  /* Wait until END_OF_CONVERSION is asserted */
   return input(P0);             /* Read ADC conversion result */
   }

/* Transmit the specified data on the serial interface */
void transmit_serial_data(unsigned char tx_data)
   {
   while (!read_bit_and_clear(TI_bit));  /* Wait until tx buffer is empty */
   output(SBUF, tx_data);                /* Read character from receiver */
   }

/* Main Execution Loop */
for (;;)
   {
   while (!read_bit(TF0_bit));  /* Wait for end of 35 mS period */
   reload_timer();              /* Reload timer with 35 mS constant */

   /* Do conversion for each repeating channel and transmit result */
   for (channel_select = 4; channel_select <= 7; channel_select++)
      transmit_serial_data(read_ADC(channel_select));

   /* Check alarm inputs to see if one of them must be reported */
   for (alarm_select = 0; alarm_select < 4; alarm_select++)
      {
      value = read_ADC(alarm_select);
      if (value != last_alarm_value[alarm_select])
         {  /* Alarm channel has changed */
         last_alarm_value[alarm_select] = value;  /* Save new value */
         if (value > ALARM_THRESHOLD)
            {  /* Transmit alarm data if it exceeds threshold */
            transmit_serial_data(alarm_select);
            transmit_serial_data(value);
            break;  /* Only one transmit allowed per 35 mS period so quit */
            }
         }
      }
   }
```

One key problem for designers is producing a design that will function properly in spite of manufacturing variations in component parameters.

vious period.

Some developers wait until the end of a project to think about which parts of a design should be tested. The problem with this strategy is that you often can't remember which parts seemed likely to need testing. By making a list of potential trouble spots as the design progresses, you can avoid this problem. The alarm-testing code fix seemed tricky enough that it would be worth testing at design-verification time, so it went on the "to be tested" list.

After the hardware prototype of the remote data-acquisition unit was built and tested, we started design-verification testing. When it came time to test the items on the "to be tested" list, it seemed like the alarm-fix test could be skipped—after all, the unit had been operating just fine in the lab. Multiple alarms seemed to be reported properly, and it was hard to believe that any real problem wouldn't have shown up by now. Nevertheless, the designer decided to proceed with testing for the alarm-blocking case.

A quick look at the possibilities of using the function generators in the lab to generate the required conditions indicated that it would not be easy to do the testing with real hardware. Getting an alarm input to alternate between two values every time it was sampled would be particularly tricky, especially since the alarm inputs are not necessarily sampled on a regular basis (the timing changes when an alarm is detected on one input). Obviously, it would be much easier to simulate than to test with real hardware.

Although SimCASE provides a built-in model for the 8051, this test required simulating the ADC as well as generating the desired waveforms for the alarm inputs. This test is not as complicated as it sounds, because it's relatively easy to combine both functions into one model using a SimI/O Program (SIOP). We modeled the ADC and alarm waveforms with the code shown in **Listings 3, 4,** and **5**. Note that SimI/O provides a skeleton SIOP, which contains the shells of all the functions presented here as well as some other necessary code (not shown). You only have to fill in the bodies of the functions.

The siopInit and siopReset functions do very little. They both initialize the variables that control the alarm waveform generation. The siopInit function also calculates the number of machine cycles needed to simulate a 50-µsec delay (used later by siopWrite).

The siopWrite function (**Listing 4**) is also quite simple. It detects transitions on the START signal and is called every time the 8051 writes to Port 1. On the rising edge of START, the SIOP clears the END__OF__CONVERSION signal, just as an ADC-0808 would. On the falling edge, it requests a 50-µsec time delay, which simulates the time required by the ADC0808 to perform a conversion. At the end of the delay, the code calls the siopTime function (**Listing 5**), which is where the interesting part of the modeling occurs.

First, the function examines the channel-select outputs on Port 1 to determine which channel is being read. A different value can be calculated for each conversion and each channel to generate any waveform desired. In this case, we used an algorithm to calculate each waveform, but it would have been just as easy to use a look-up table to generate arbitrary waveforms (an example is given later). Alternatively, we could

LISTING 2—REVISED ALARM-CHECKING ROUTINE, USING ROUND-ROBIN PRIORITIZATION

```
/* Check alarm inputs to see if one of them must be reported */
for (count = 4; count--;)  /* Execute loop four times */
    {
    value = read_ADC(alarm_select);
    if (value != last_alarm_value[alarm_select])
        {  /* Alarm channel has changed */
        last_alarm_value[alarm_select] = value;  /* Save new value */
        if (value > ALARM_THRESHOLD)
            {  /* Transmit alarm data if it exceeds threshold */
            transmit_serial_data(alarm_select);
            transmit_serial_data(value);
            break;  /* Only one transmit allowed per 35 mS period so quit */
            }
        }
    if (++alarm_select > 3)    /* Increment alarm select and */
        alarm_select = 0;      /* wrap around to 0 if necessary */
    }
```

NOTE: Shading indicates the changed lines of code

LISTING 3—INITIALIZATION CODE FOR THE ADC SIMULATOR PROGRAM

```
unsigned int last_P1, last_channel_1, last_channel_2;
long conversion_delay;

/* This function is called when the SIOP is initially mapped in */
int siopInit(
            byte Seg,                  /* Segment SIOP is mapped to */
            word Addr,                 /* Address SIOP is mapped to */
            byte Dir,                  /* Direction SIOP is mapped */
            char *P_Id,                /* SIOP identifier */
            int (*(*P_Fcn)[])(),       /* Pointer to the SimCASE function pointers */
            struct sysdata *P_SysData  /* Pointer to SimCASE global variables */
            )
    {
    /* Save the SimCASE system pointers */
    P_simCASEFcn = P_Fcn;
    P_Identifier = P_Id;
    P_SystemData = P_SysData;
    /* Calculate the 50 microsecond conversion delay in machine cycles */
    conversion_delay = (50L * P_SystemData->Clock) / 12000L;

    /* Initialize SIOP state variables */
    DATA_READ(&last_P1, SFR_SEG, P1_ADDR);
    last_channel_1 = 120;
    last_channel_2 = 200;
    return OK;
    }


/* This function is called whenever the 8051 is reset */
int siopReset(byte Seg, word Addr, byte Dir)
    {
    /* Initialize SIOP state variables */
    DATA_READ(&last_P1, SFR_SEG, P1_ADDR);
    last_channel_1 = 120;
    last_channel_2 = 200;
    return OK;
    }
```

LISTING 4—DATA-WRITE CODE FOR THE ADC SIMULATOR PROGRAM

```
/* This function is called whenever the 8051 writes to Port 1 */
int siopWrite(
               word Data,   /* Data written by the 8051 program */
               byte Seg,    /* See siopInit */
               word Addr    /* See siopInit */
               )
    {
    /* Test for rising edge on START output */
    if (((Data & 0x08) != 0) && ((last_P1 & 0x08) == 0))
       {  /* Rising edge on START detected */
       DATA_WRITE(0xEF, PSEUDO_SFR_SEG, IP1_ADDR);  /* Clear END_OF_CONVERSION */
       }
    /* Test for falling edge on START output */
    if (((Data & 0x08) == 0) && ((last_P1 & 0x08) != 0))
       {  /* Falling edge on START detected */
       TIME_DELAY(P_Identifier, conversion_delay);  /* Start 50 uS time delay */
       }
    last_P1 = Data;  /* Save last P1 value */
    return OK;
    }
```

For many types of components, the worst-case timing will occur only under extremes of temperature and supply voltage, both of which may be hard to reproduce.

have used a randomizing function to generate a random waveform.

The equations in **Listing 5** return fixed values for analog inputs 0, 3, 4, 5, 6, 7 (the value is the channel number plus 10). The code causes analog input 1 to alternate between values 120 and 121, and analog input 2 to start with a value of 200 and increment on each reading. Because the alarm threshold is 100, both channels 1 and 2 should generate a constant stream of alarms. After calculating the conversion result, the code simulates the ADC0808's output by writing the result to the Port 0 inputs of the 8051; the code asserts the END__OF__CONVERSION signal by writing to the Port 1 inputs of the 8051.

Running the test

After compiling the SIOP, we started SimCASE, loaded the operational code for the remote data-acquisition unit, and mapped the SIOP to the control port (Port 1). To simplify viewing the results, we arranged to display the last 12 bytes transmitted on the serial interface by specifying that ?SERBUF (for the 8051 serial port) be displayed in the user window. By single-stepping the code through several conversions, we saw that the SIOP was operating properly—each conversion required 50 μsec to complete, and the expected results were produced. Unfortunately, the data-acquisition unit was not acting properly. The resulting SimCASE screen is shown in **Fig 3**.

In spite of the fix, which was installed to prevent a constant alarm on one channel from blocking other alarms, the data-acquisition unit was only reporting the alarm on channel 1—it had a bug. Using SimCASE to trace through the code, it was easy to determine that the problem was in the placement of the code that updated alarm__select. The conditional statement:

```
if (+ +alarm__select > 3) /* Increment alarm select and */
   alarm__select = 0; /* wrap around to 0 if necessary */
```

was incorrectly placed at the end of the alarm testing loop—where it was never executed if an alarm was detected. The result was that the code would always resume testing alarms with the last reported alarm. By moving these two statements to the beginning of the loop, the code worked properly. After modifying the operational code, it was easy to repeat this test and verify that the revised code functioned as expected.

One key problem for designers is producing a design

LISTING 5—TIME-DELAY CODE FOR THE ADC SIMULATOR PROGRAM

```
/* This function is called when a previously requested time delay expires */
int siopTime(void)
    {
    unsigned int result;
    unsigned int channel;

    /* Select conversion value to return based on channel select outputs */
    channel = last_P1 & 0x07;
    if (channel == 1)
        {  /* Analog channel 1 */
        if (last_channel_1 == 120)  /* Alternate between 120 and 121 */
            result = ++last_channel_1;
        else
            result = --last_channel_1;
        }
    else if (channel == 2)
        {  /* Analog channel 2 */
        result = ++last_channel_2;  /* Increment by one each time its read */
        }
    else
        {  /* Analog channels 0, 3, 4, 5, 6, 7 */
        result = channel + 10;  /* Return the channel number + 10 as a dummy */
        }                       /* result for most channels */
    DATA_WRITE(result, PSEUDO_SFR_SEG, IP0_ADDR);  /* Output result to Port 0 */
    DATA_WRITE(0xFF, PSEUDO_SFR_SEG, IP1_ADDR);  /* Set END_OF_CONVERSION */
    return OK;
    }
```

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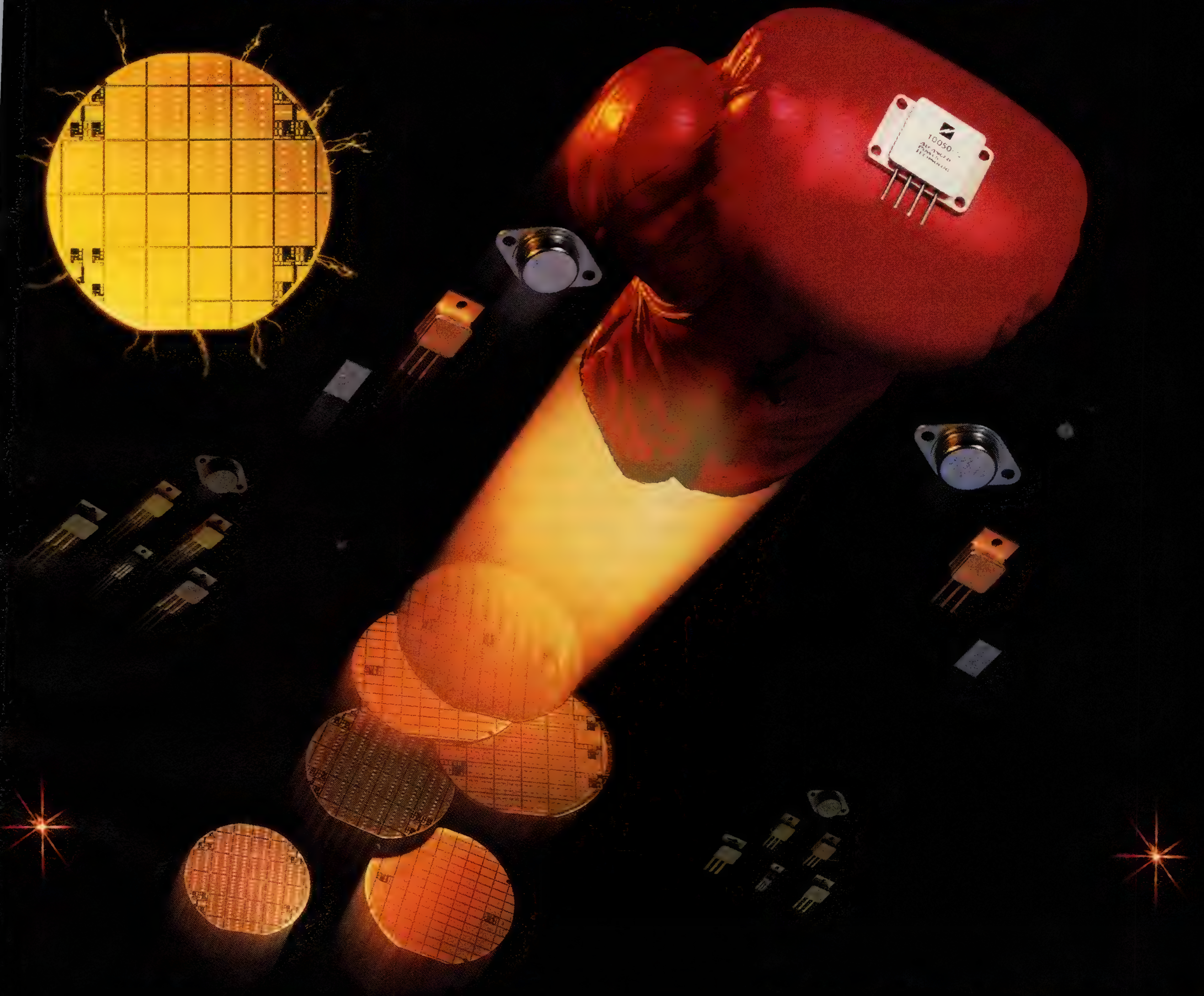

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0.20 - 1.30	26.0 - 8.5	104 - 34	1800 - 2950	60 - 130	0.414 × 0.254 (106)
0.30 - 2.40	18.5 - 5.0	74 - 20	1300 - 1800	45 - 105	0.290 × 0.250 (105)
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Regression testing is good for a designer's peace of mind, but it is often omitted because it can consume an unacceptable amount of time.

that will function properly in spite of manufacturing variations in component parameters. For products that are produced in volume, you may need to consider how much a critical component's parameters will vary from one purchase lot to the next—especially if you purchase the same part from more than one vendor. Even if you plan to produce only small quantities of a system, you should consider the variations that may occur because of changes in the product's operating environment (such as ambient temperature, humidity, and power-supply voltage) or because of component aging.

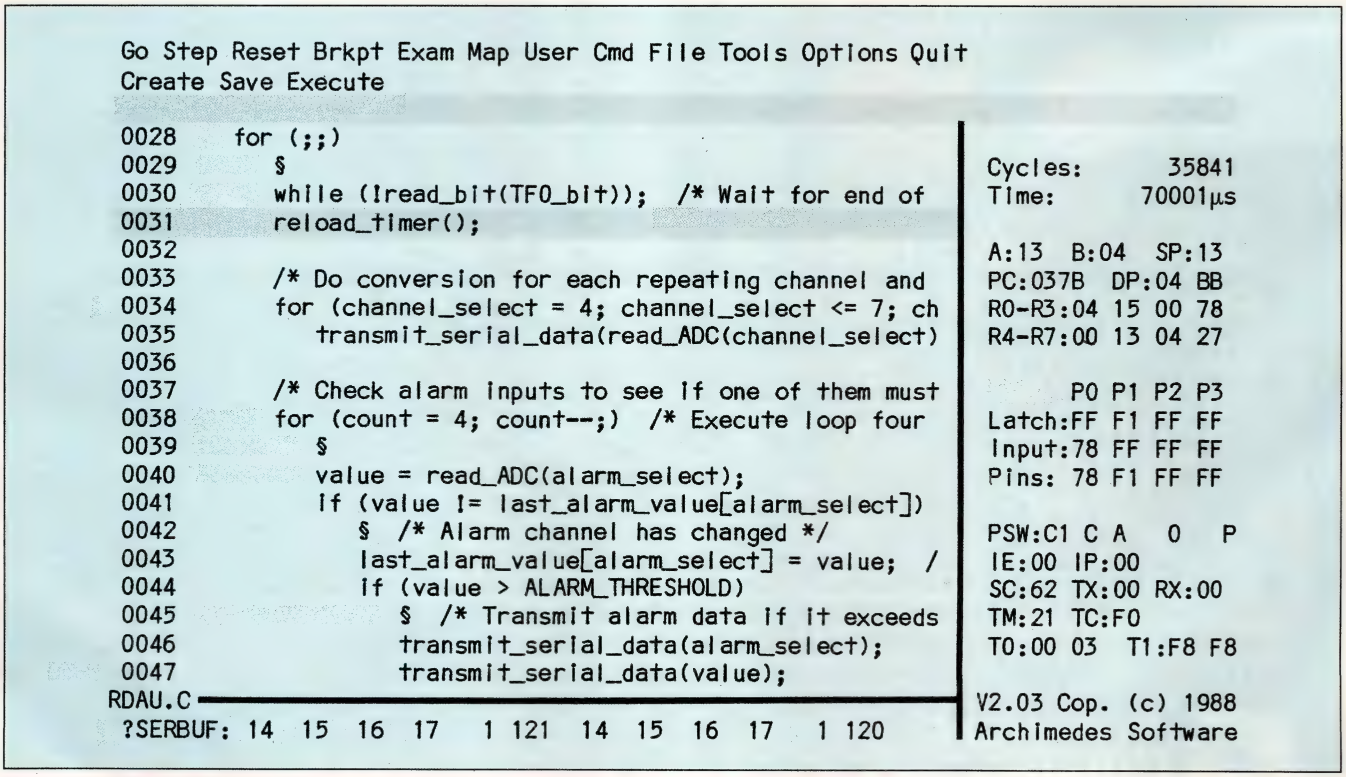
Such concerns typically fall in the domain of hardware designers, but software developers must also be concerned if their code depends on hardware parameters that are subject to these same variations—especially in the case of microcontroller code, which often deals with hardware on a low level. Some examples of timing that might vary from unit to unit or change with aging include

- The activation time required to close a relay
- The time required for a disk drive to complete a seek
- The delay before a programmable-power-supply output is stable
- The conversion time for an ADC
- The program or erase time for an EEPROM.

A change in the timing generated or required by a component can have many effects. The simplest, and most obvious, is that the component ceases to operate because its operating requirements have not been met. Changes in timing can also stress the software design. A hardware component that operates faster or slower than its specifications can force software to process events in a different order than that required by the specified speed. This new order may produce a sequence of events that you could not foresee.

Changes in hardware timing may also exercise limiting cases in the software that you would not otherwise encounter. For example, a software timeout counter for a 30-msec (maximum) disk-seek operation that uses the following (invalid) code would operate properly with all disk-drive units requiring 29 msec or less to perform a seek, but would fail with those units requiring the full 30 msec called out in the disk drive's specifications.

```
if (+ +timer < 30)
   timeout__error();
```



```
Go Step Reset Brkpt Exam Map User Cmd File Tools Options Quit
Create Save Execute

for (;;)
   §                                                    Cycles:       35841
   while (!read_bit(TF0_bit));  /* Wait for end of      Time:       70001µs
   reload_timer();
                                                        A:13  B:04  SP:13
   /* Do conversion for each repeating channel and      PC:037B  DP:04 BB
   for (channel_select = 4; channel_select <= 7; ch     R0-R3:04 15 00 78
      transmit_serial_data(read_ADC(channel_select)     R4-R7:00 13 04 27

   /* Check alarm inputs to see if one of them must           P0 P1 P2 P3
   for (count = 4; count--;)  /* Execute loop four      Latch:FF F1 FF FF
      §                                                 Input:78 FF FF FF
      value = read_ADC(alarm_select);                   Pins: 78 F1 FF FF
      if (value != last_alarm_value[alarm_select])
         §  /* Alarm channel has changed */             PSW:C1 C A   0   P
         last_alarm_value[alarm_select] = value;  /     IE:00 IP:00
         if (value > ALARM_THRESHOLD)                   SC:62 TX:00 RX:00
            §  /* Transmit alarm data if it exceeds     TM:21 TC:F0
            transmit_serial_data(alarm_select);         T0:00 03  T1:F8 F8
            transmit_serial_data(value);
RDAU.C                                                  V2.03 Cop. (c) 1988
?SERBUF: 14  15  16  17   1 121  14  15  16  17   1 120 Archimedes Software
```

Fig 3—This SimCASE screen is one of a series *showing that the alarm select loop was operating incorrectly.*

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Design-verification testing is a necessary part of any serious microcontroller-product development.

Vendors are seldom able to provide you with hardware units that exhibit worst-case timing behavior. Even units that barely squeak through the manufacturer's quality-assurance tests will rarely exhibit exactly the characteristics that you need for test purposes. Furthermore, for many types of components the worst-case timing will occur only under extremes of temperature and supply voltage, both of which may be difficult to reproduce. Thus, it's hard to set up a worst-case testing program that will use real hardware. Fortunately, you can simulate worst-case timing just as easily as typical timing.

Play it again, Sam

You may be tempted to think that your design-verification tests are no longer useful when you've finished the design-verification phase of your project—but don't discard them yet. Many developers like to run their suite of design verification tests after each major revision of a product's operational code. Such "regression testing" can ensure that a modification in one part of the code didn't break something in another part of the code. How many times have you added "just one more little feature," only to find out later that it pushed the size of the instruction code past the end of available ROM, or modified a variable used by another routine?

Although regression testing is good for the designer's peace of mind, it is often omitted because it can consume an unacceptable amount of time. This is especially true if it requires you to set up complex hardware test configurations and instrumentation all over again. Simulated design-verification tests have an advantage here because they do not require such configurations.

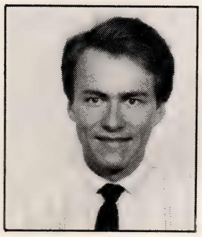
Like tests using real hardware, simulated tests still require that the developer review the test results to determine if there are problems. If tests are constructed so that a number of manual modifications and inspections are required, the testing process can be quite tedious. Fortunately, you can dramatically reduce the retesting effort by structuring the tests properly and adding a few carefully chosen statements. Here are some suggestions:

- Use command files to set up display variables and execute the tests. Such files make it simpler to run the test at a later time when the operation of a test SIOP is not as fresh in your mind.
- Where possible, have the SIOP code, not the operator, measure characteristics such as pulse widths and time delays. Use the ERR__MSG function to display the result of such measurements on the status line.
- If the "correct" outcome for a test is easily identifiable (a known pulse width must be produced or a particular signal must be asserted), have the SIOP display a PASS or FAIL message. This eliminates the time required by the operator to evaluate the outcome.
- Use a single command file to initiate a whole series of tests, and log the results of each test to a disk file, using the file read/write capabilities of the SIOPs.

Although these techniques will not reduce the amount of computer time required to rerun the design-verification tests, they can reduce the amount of time the developer has to spend on them. Regression testing can be simply a matter of starting the tests one evening and reviewing the results the next morning.

Design-verification testing is a necessary part of any serious microcontroller-product development; it is especially critical for applications such as medical instruments, industrial controllers, and military products. However, the available time and resources often limit the amount of testing you can actually perform. Simulation provides a cost-effective way to perform many design-verification tasks. You should seriously consider simulation if you need to test your application under a variety of conditions that are difficult to generate or that have unlikely sequences of events, hardware malfunctions that exercise built-in diagnostic code, or timing variations due to hardware tolerances. EDN

Author's biography



Anders Gezelius is the president of Archimedes Software Inc, designers of software-development tools for microcomputers and microcontrollers. Anders holds an MS in electrical engineering from the Royal Institute of Technology in Stockholm, Sweden, and an MBA from the Wharton Business School in Philadelphia, PA. In his spare time he enjoys skiing, and he finds that studying world history is a humanizing counterbalance to the rigors of the technical world.

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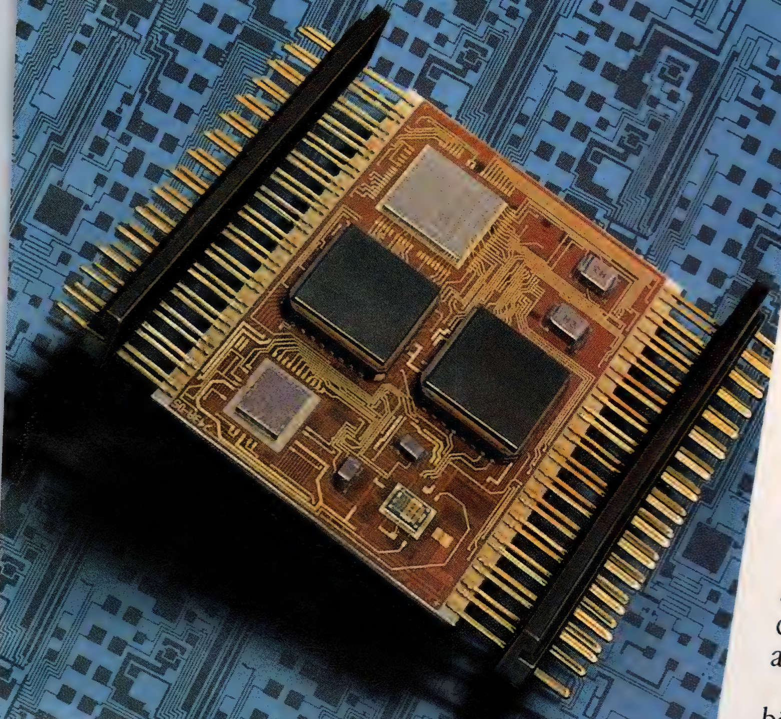

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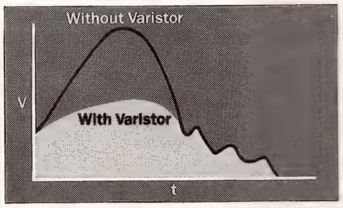

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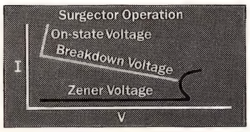

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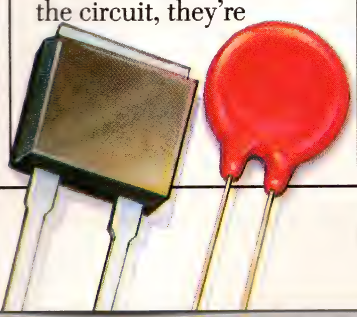

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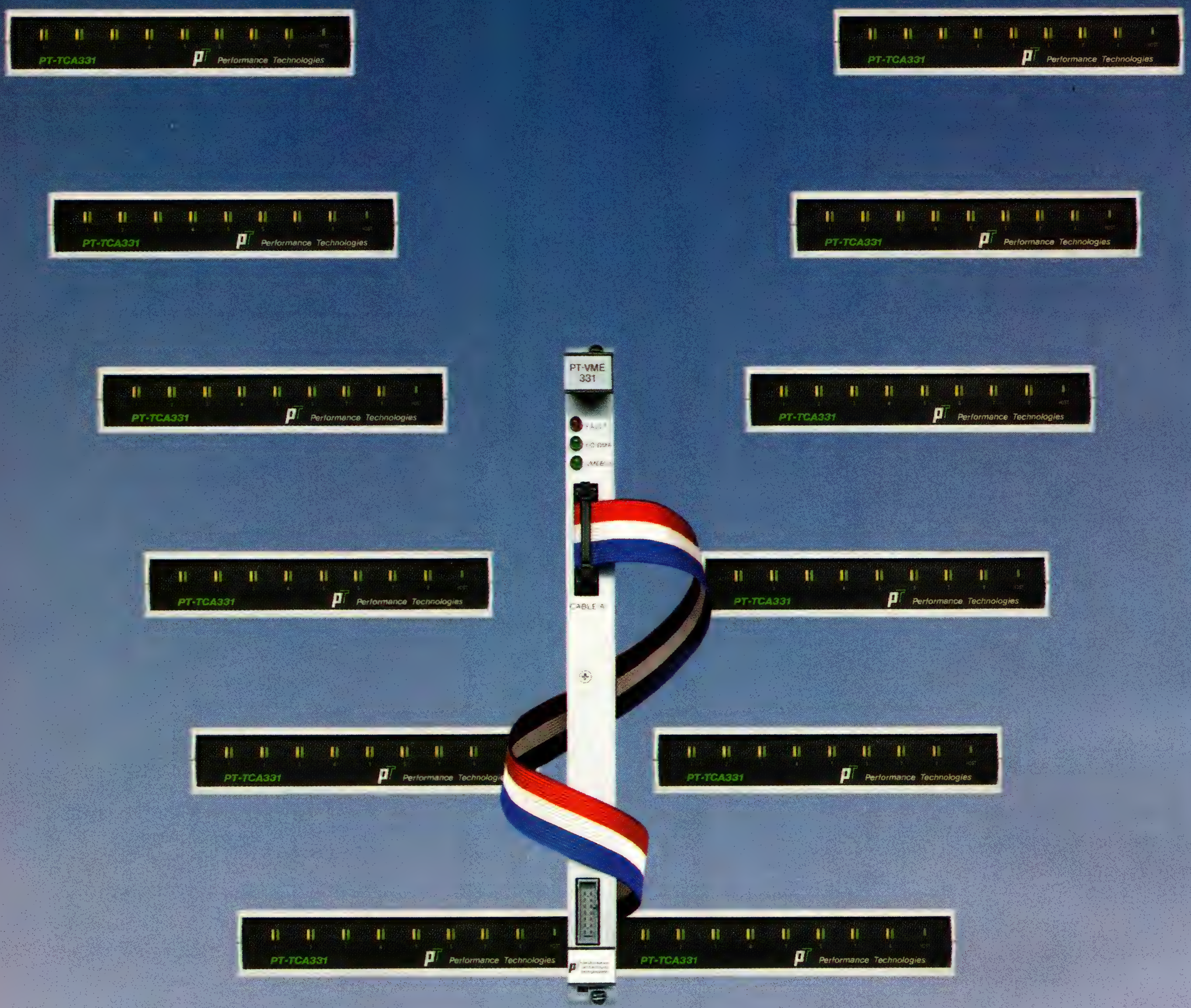

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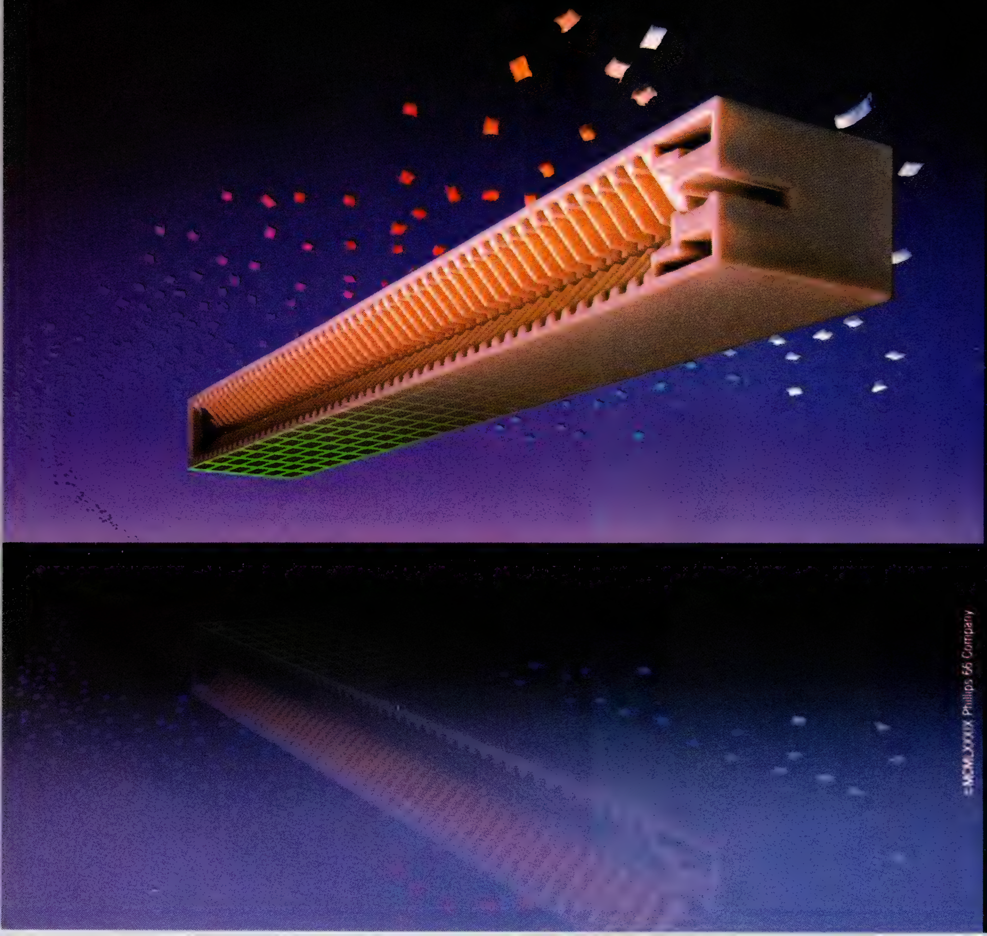

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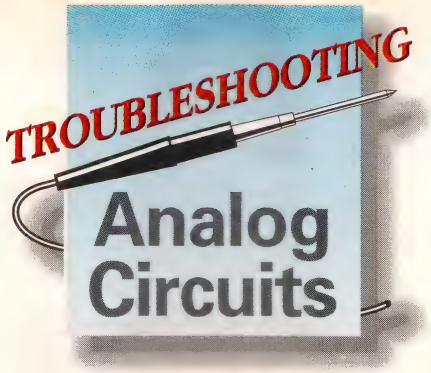

PART 11

Preside over power components with design expertise

Bob Pease—the self-appointed Czar of Band Gaps—continues his series with words of wisdom on voltage references, regulators, and start-up circuits. He also warns against assumptions about worse-case conditions and discusses the usefulness of Kelvin connections. Next time, Bob wraps up this series with some final remarks about troubleshooting.

Robert A Pease, *National Semiconductor Corp*

Voltage references and regulators have internal features that make them somewhat immune to problems. But, as with other designs, if you ignore the details, you'll be headed for Trouble. Some designs incorporating these parts, such as switching power supplies, are not for the novice.

Many voltage references are based on band-gap circuitry, but some of the best references are based on buried zener diodes. If your power supply's output is in the 8 to 12V range, zener-diode references can provide high stability, low noise, and a high temperature coefficient. If your power-supply output is a lower voltage, you can find band-gap references that put out anywhere from 0.2 to 5V with creditable efficiency and economy. These band-gap references feature as high a temperature coefficient as you'd probably ever be willing to pay for. But they also feature enough noise so that a little filtering makes a big improvement.

A good buried-zener-diode voltage reference is inherently more stable over the long term than is a band-gap one—zener designs change only 5 to 10 ppm per month. However, if you want the highest stability possible, it's only fair to age, stabilize, and burn-in zener-diode devices first. Also, you must screen out the ones that just keep "walking" away from their set points 10 to 20 ppm every week—there are always a few "sports" that are driftier than the rest. Unfortunately, there's no quick and easy test to distinguish between the drifty ones and the stable ones, except for taking measurements for many hundreds of hours.

Regulators are *almost* foolproof

In the last 10 years, IC voltage regulators have gotten pretty user friendly. Many people use them with no problems at all. Still, my colleagues and I get at least one call every month about a regulator working poorly. The indignant caller complains, "It's getting hot." We ask, "How big is your heat sink?" The indignant voice responds, "What do you mean, heat sink?" I credit all of you readers with enough smarts to recognize that you can't put a whole lot of power into a little regulator unless you secure it to a sufficient heat sink or fins. Then, there really aren't too many things that are likely to go wrong because voltage regulators have

Once you realize that you can't put a whole lot of power into a little regulator unless you secure it to a heat sink, not much is likely to go wrong.

just about every feature for protection against the world's assaults.

You'll have problems with regulators when you don't provide the proper output filtering. Most negative regulators and some other types, such as low dropout regulators, require an electrolytic bypass capacitor from the output to ground. If you insert a tantalum capacitor, you may be able to get away with a value of 1 or 2 μF; if you use an aluminum electrolytic capacitor, you can get away with 20 to 100 μF. But in all cases, an electrolytic capacitor WILL work, and a film or ceramic capacitor WON'T work—its series resistance is just too small. If you put a 1Ω resistor in series with a 1-μF ceramic capacitor, the filtering will be adequate at room temperature, but at −40 or +100°C, the capacitor's value will shrink badly.

Another regulator problem can occur when you add an external transistor to increase the output current. Since this transistor adds gain at dc, it's not surprising that you have to add a bigger filter capacitor on the regulator's output to prevent oscillation. Some of the applications in National Semiconductor data sheets recommend specific values for the filter capacitor, but some of these circuits are quite old. When customers find out that 2N3234s are no longer available, they're likely to substitute a more modern transistor that has a faster response and is likely to oscillate. In this case,

Photographs by Peggi Willis

When you're "Czar of Band Gaps," *people look up to you.*

What is worst case?

Once I designed a circuit to drive a 200Ω load at the far end of a 2000-ft RG174U cable. The specifications called for me to test the circuit by driving the near end of the coaxial cable with a low-impedance square wave. I called the engineer who wrote the spec and recommended that we perform the test with about a 39Ω source impedance to avoid bad ringing and reflections along the unterminated cable. He told me that this impedance wasn't necessary; he had already checked out the worst-case conditions with no cable and with 2000 ft of cable. I asked him if he had checked it with 250 ft of cable. Why no, he said. So I suggested he try that.

Shortly thereafter, he called me and agreed that the reflections with 250 ft of cable were intolerable without at least some nominal value of resistance at the source. He had incorrectly assumed that the worst case occurred with the longest cable. It's true that the attenuation was worst with the long length of lossy RG174U cable. But it was this attenuation that caused the ringing and reflections to appear damped out. With the shorter cable, a worst-case condition existed at a place he hadn't expected to find it.

So, be cautious about where you look for worst-case conditions. An op amp may exhibit its worst performance at an output voltage other than its maximum negative or positive swing—or even other than zero volts or zero output current. A regulator's worst-case operating conditions may not be at its full-rated load current. When a regulator's power source is resistive, the power dissipation may be higher at three-quarters of its rated current than at full current.

Once I worked on a regulator

a customer might complain about the dc output's "bad stability" as the regulator is forced into and out of oscillation. (Whoever said you don't need an oscilloscope to check out dc problems?) When these customers ask for help, I not only explain how to stop the oscillation, but I give them Pease's Principle (see the **box**, "Pease's Principle," on page 138 of the September 1, 1989, issue of EDN).

Too much voltage leads to regulator death

You CAN kill any regulator with excessive voltage. So if you're driving inductive loads or your circuit has an inductive source, make sure to have a place for the current to go when the normal load path changes. For example, if you're using the LM350 as a battery charger with only a few microfarads on the input, a short between the output and ground is disastrous. When the regulator tries to draw an increasing amount of current from the transformer and then goes into current limit, you can get marvelous 80V transients, which destroy the LM350. The solution is to put 1000 µF—rather than just 1 or 10 µF—across the input.

Users get accustomed to seeing regulators with output noise of about 0.003% of the rated dc output. They get indignant when the noise doubles or triples due to 1/f or popcorn noise. The chances of finding a noisy regulator are quite small, so when some noisy ones DO show up, it's a shock. Unfortunately, no high-volume manufacturer of regulators is in a position to test for those low noise levels or guarantee that you'll never see a noisy part. Please don't expect the manufacturer to admit the parts are bad or unreliable or worthy of being replaced. If you DO depend on super-quiet ICs, it's wise to keep a spare stock of selected and tested parts in a safe. Then, you can find them when the ones you just bought end up being a little too noisy.

These simple tips aren't meant to overshadow the truly difficult areas of regulator design. You might wonder if it's possible for a smart, experienced engineer to design a switch-mode regulator that works well after only minor redesigns and goes into production without a major yield loss. My answer is, just barely. The weasel word here is "smart." If the engineer forgets some little detail and doesn't have a contingency plan to test for it, screen it, or repair the regulators that don't work, then maybe he or she isn't very "smart." Those of us who don't design switchers all the time would have a very poor batting average at getting a design to work right off the drawing board—even if we're really good at designing other circuits. After all, a switcher is a complicated system composed of power transistors, transformers, inductors, one or more control ICs, and lots of other passive components. And, the circuit's layout is critical. The

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that ran okay at −55°C, at room temperature, and at +125°C, but not at some intermediate temperatures. That was a nasty one. Because some engineers had tested the regulators at hot and cold temperatures and saw no trouble at these extremes, I had to work very hard to convince them not to ship these parts. I had to take them by the hand and show them where the trouble was. It's like a dumb cartoon I once saw showing three men walking out of a movie—an old man, a young man, and a middle-aged man. The posters said the movie was "fun for young and old." And sure enough, the old man and the young man were smiling, but the middle-aged man was frowning. Even a dumb cartoon can be instructive if it reminds you that bad news is not only where you first expect it. It may be lurking in other places, too.

This story reminds me of a boss who asked me if my new regulator design was really short-circuit proof. I told him, yes, I had tested it with short bursts and long pulses and everything in between for days and weeks. With a wry smile, he went over to a tool cabinet and removed a really big, heavy file. He applied this file with rough, uneven scraping motions to ground and to the output of my regulator. He got showers of sparks out of the regulator, but he couldn't kill it. Then he explained to me that the random, repetitive action of a file sets up patterns of current loads and thermal stresses that can kill a regulator if its short-circuit protection is marginal. There are many, many tricks you can use to show that a design really can survive every worst-case condition.

Many regulators require electrolytic capacitors on their outputs; ceramic ones simply don't do the job.

layout must guard electrostatic signals and, even more importantly, electromagnetic strays. The paths for high currents are important, and the paths for cooling air are even more critical.

So when someone asks me how to design a switcher, I ask, "How many do you plan to build?" If the answer is a few dozen and the design is a full-featured high-power job, I encourage the engineer to buy an existing design. But if large volumes are involved, an engineer usually has the time to do the design right and spread that effort over a few thousand circuits.

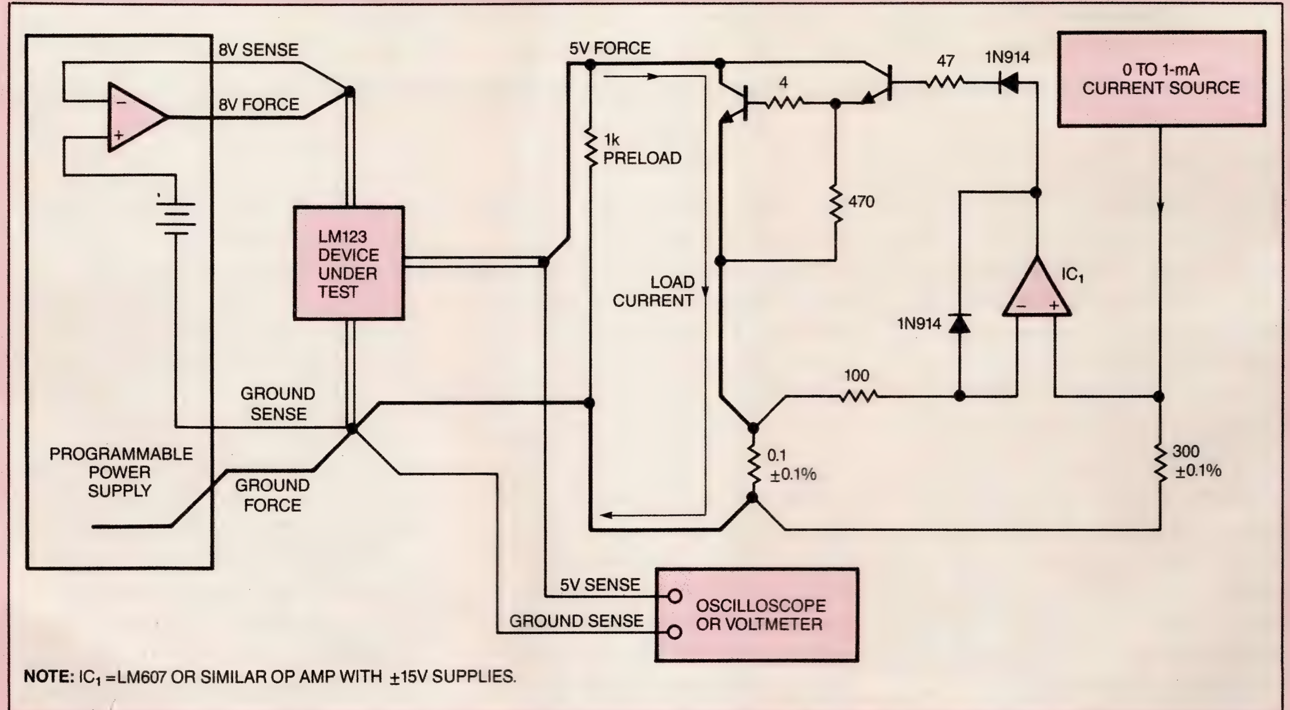
An alternative to designing your own switcher is using one of a number of small but complete switching-regulator ICs. Some of these chips are about as foolproof—for a switcher—as you can get. You may need a couple resistors, a few capacitors, an inductor, and a fast rectifier, and then it's done. You'll have a cookbook circuit that really does work. If you only need to supply a few hundred milliamps to your circuit, you may not even need a power transistor or a heat sink.

Kelvin connections improve measurement accuracy

The usefulness of Kelvin contacts and connections is not widely appreciated. In fact, when I received a question about them recently, I found very little printed reference material on the subject. I looked in a few dozen reference books and text books and didn't find a definition or explanation anywhere. I did find some "Kelvin clips," which facilitate Kelvin connections, in a Keithley catalog. I also found some Textool socket data sheets, which mentioned, in a matter-of-fact way, the advantages of Kelvin contacts. I'll try to explain their usefulness in more detail here.

Perhaps the most common use of Kelvin connections is the remote-sense technique. Kelvin connections and sockets let you bring a precise voltage right to the terminal or pin of your circuit under test. If you don't control the supply voltage precisely, you might start failing parts that are actually meeting their specs.

For example, let's say we want to test the load regulation of the



NOTE: IC_1 =LM607 OR SIMILAR OP AMP WITH ±15V SUPPLIES.

***Fig A—By using Kelvin connections** you can avoid measurement errors caused by IR drops in the circuits that you're trying to measure. In this circuit diagram, there are four pairs of Kelvin connections.*

Even in the last couple years there have been advances in designs that really do work, as opposed to paper designs that have no chance of surviving a short on the output or of working under worst-case conditions. Although a few of these useless paper designs still pop up from time to time, thank heaven that most of them have been driven out.

One of the stories that keeps rattling around the industry is about a group of engineers who decide to band together and start a new computer company. The smartest one is assigned to do the main processor board. Another smart engineer does all the interfaces. And the smart but green "kid engineer" is assigned to do the switch-mode power supply because, of course, that's the easiest part to do. (Anybody who has worked on a big switcher will probably speak up right away: The switcher is NOT as easy as it seems.) In the end, the power-supply design takes a lot longer than everybody expects.

One day, the young engineer opens up the compart-

LM323, a 5V regulator, when $V_{IN}=8V$ and the load changes from 5 mA to 3A (**Fig A**). In this circuit, there are four pairs of Kelvin connections shown. The first pair is located at the power supply's output. This programmable supply's remote-sense terminals permit it to maintain an accurate 8V output right up to the pin of the device under test (DUT).

The second Kelvin connection in **Fig A** is located at the output of the DUT. In order for you to observe the changes in V_{OUT} as you apply various loads, the Kelvin contacts provide force leads for the 3A of output current. They also provide sense leads, so you can observe the DUT's output with a high-impedance voltmeter. Note that there are two sense and two force connections to the ground pin of the DUT. You don't really need all four contacts—you can tie both force leads and both sense leads together.

The op amp in **Fig A** forces the DUT's output current through the Darlington transistor and then through a 0.1Ω precision resistor. The only way to use a 0.1Ω resistor with any reasonable accuracy and repeatability is to use the 4-wire connections as shown. The op amp can force the upper sense lead to be precisely 300 mV above the lower sense level, even if the lower end of the resistor does rise above ground due to various IR drops in wires or connectors.

There are several places in this circuit that we could call ground, but the only ground we can connect to the 300Ω resistor and get good results with is the sense lead at the bottom of the 0.1Ω resistor. If you connect the bottom of the 300Ω resistor to any other "ground," shifts in the IR drops would cause relatively large and unpredictable shifts in the value of the 3A current—in other words, Trouble. So, when you're running large currents through circuits, think about the effects of IR drops in various connectors and cables. If you think IR drops will cause trouble, maybe Kelvin connections can get you out of it.

Fig A's fourth Kelvin connection is hidden inside the 5V regulator, which has separate force and sense connections to the output terminal. A fifth Kelvin connection is also concealed inside the current-limit circuitry of the regulator. Here, the device senses current with a 4-wire, Kelvin-connected resistor before the current goes to the current-limit sense amplifier.

The use of Kelvin sockets is not confined to large power transistors or high-current circuits. Consider a voltage reference with 2 mA of quiescent current. If you're trying to observe a 1-ppm stable reference and the ground connection changes by 5 mΩ (which most socket manufacturers do not consider disastrous), the 10-μV shift that results from this change in ground impedance could confound your measurements. If you want to avoid trouble in precision measurements, avoid sockets or at least avoid sockets that do not have Kelvin contacts. Lord Kelvin—William Thomson Kelvin before he was appointed a baron—did indeed leave us with a bag full of useful tools.

It's just barely possible for an experienced engineer to design a switching regulator that works well the first time out.

ment where the power supply resides, and it blows up in his face. After his coworkers take the poor fellow to the hospital, they ask around and find a consulting engineer who makes a living out of fixing exactly this kind of switcher problem. The switcher design was slightly off-course and needed the hand of an expert before it would work correctly. So remember, designing switchers is no simple task. Don't hesitate to call in an expert.

Regulators suit different power levels

There are several different configurations of switch-mode regulators. At low power levels, capacitively coupled switcher designs are simpler but don't provide much choice of V_{OUT}: $1.9 \times V_{IN}$, $-0.9 \times V_{IN}$, and $0.45 \times V_{IN}$ are almost the only choices. Flyback regulators are the simplest and cheapest magnetically coupled regulators. However, at power levels above 100W, their disadvantages become objectionable, and forward or push-pull schemes are more popular. At the highest power levels, bridge-type designs are best. If you try to use a configuration at an inappropriate power level, you may have to struggle to get it working. Likewise, the use of current-mode regulation may help you get faster loop response, but the concept is difficult to understand, let alone execute.

Current limiting is always a problem with switchers. The choice of a sense resistor is not easy because the resistor must have low inductance. As with most aspects of switch-mode regulation, to achieve marginal reliability and to avoid trouble, you have to spend the time to design and test the current-limiting circuit carefully.

Similarly, a soft-start circuit is important for a large switcher, especially when the switcher strains to put out a lot of current to quickly charge up the output filter capacitors. For a large supply, this current could damage transistors, wires, fuses, and power companies. A soft-start circuit forces the switcher to bring the output up to its working levels gradually. I could show you a good soft-start design, but I'll do better than that—I'll show you a bad one. The LM3524 data sheet shows the circuit in **Fig 1** for a 15V, 0.5A step-up switching regulator. (I should mention that this circuit and the LM3524 data sheet were mistakenly left out of National Senmiconductor's 1986 data book. We plan to reinsert them in future editions.)

A step-up switcher needs a soft-start circuit to pre-

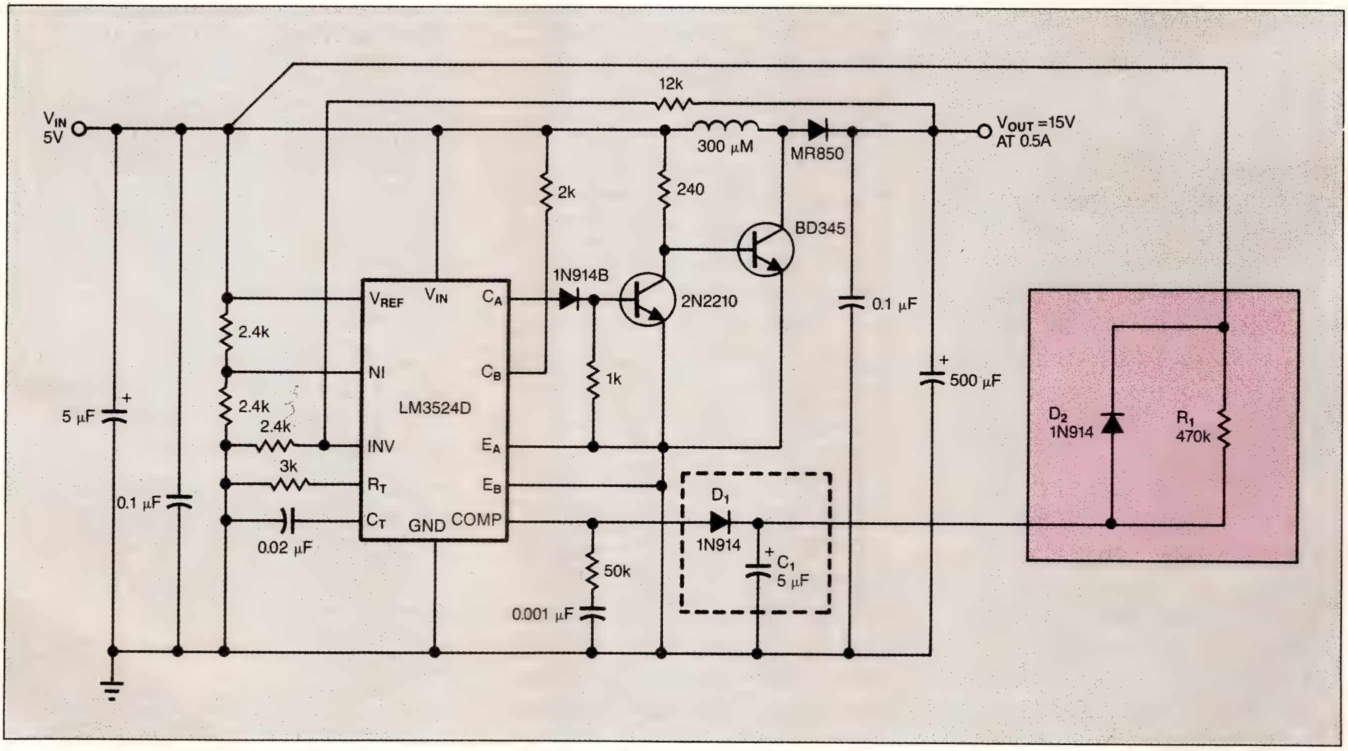


***Fig 1—The addition** of R_1 and D_2 to this standard data-book design of a 15V, 0.5A switching regulator provides the circuit with better soft-start and restart capabilities.*

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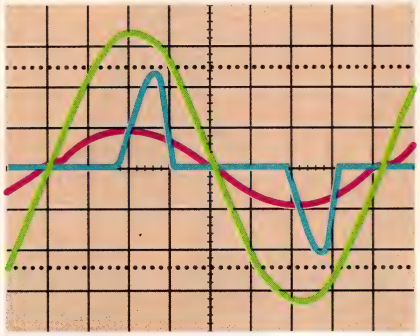

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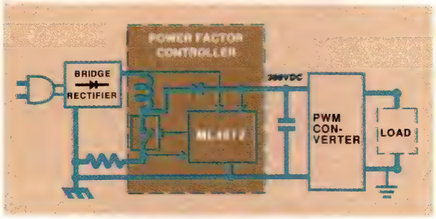

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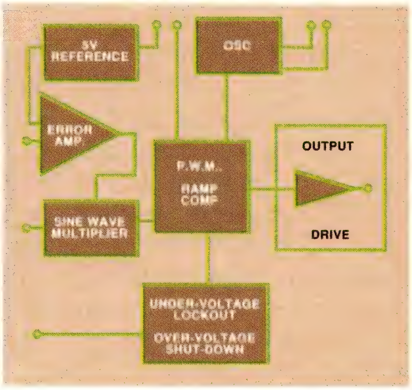

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Anyone who has ever worked on a large switching regulator will tell you that designing them is no trivial task.

vent it from saturating its transformer and from just sitting there at start-up. For this reason, C_1 and D_1 were included in **Fig 1**'s circuit. But **Fig 1** is still a bad circuit. Let's say that the regulator is running at a low duty cycle and the voltage on the COMP pin is relatively low. Now, as the input voltage changes, the duty cycle may have to increase. But the control amplifier that drives the COMP pin not only has to pull up the series RC network at the COMP pin, but it must also pull C_1 up to the new voltage level. This load is too much for the COMP pin's control amp. It's possible to avoid this problem by adding a 470-kΩ resistor from the top of C_1 to the input supply. This resistor pulls C_1 up to a high level, where it cannot interfere with operation after start-up.

Even after you add the resistor, this circuit is in trouble—especially if the input power shuts off briefly. It takes many seconds to discharge C_1, a 5-μF capacitor, and after a brief power outage no soft-start capability will be available. A good fix is to install a diode across the 470-kΩ resistor to discharge C_1 quickly when the input voltage drops. This gives you a chance for soft start on the restart. I'm not saying that this circuit is a good worst-case design—you'd have to prove that with engineering and tests. Meanwhile, we'll have to add these components to our LM3524 data sheet.

Toys illustrate some basics

My first encounter with a start-up circuit happened at a pretty young age. I remember the old toy that resided in a box with a big ON-OFF toggle switch on its front. When your curiosity led you to flip the switch ON, a motor would begin to whir, the top of the box would rise up, and a mechanical hand would reach out. The hand would throw the switch to the OFF position and then retreat back into the box. The cover would close, and the whirring would cease. What a charming way to represent a start-up (or, in this case, a shut-down) function. When I was a kid, I was really impressed by this toy, but later I realized that this logical sequencer was an illusion. The ON-OFF switch DID trigger some kind of a latch to turn the power ON, but it did not directly provide the OFF function. If it did, the hand would stall immediately after it turned the switch OFF and would never continue back inside the box. There was a switch to turn the power OFF, but it was functionally inside the box at the end of the travel of the hand.

The point of the story is that we must make sure not to fool anybody with the start-up circuits we design. When I design an A/D converter, I include a shift-register sequencer to make sure that every necessary task is completed sequentially at the start of conversion and again at the end. I have no idea how software engineers write valid programs to make sure no false start-up sequences occur, but I bet some people do it wrong. Some designs still implement the microprocessor reset function with such crude RC timers that the processor gets confused and doesn't start correctly. I've heard about those horror stories. Sometimes people forget to add the diode to discharge the capacitor, and then the reset fails to work after a brief power outage.

Designers also include start-up circuits in linear circuits. For example, current-bias circuits ensure that a small but stable bias current starts the whole circuit going. Then when the start-up circuit is operating

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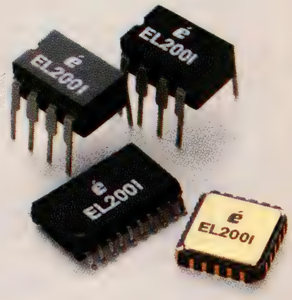

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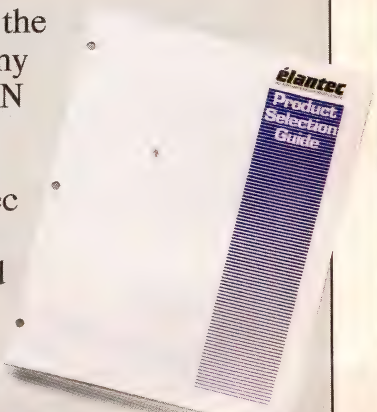

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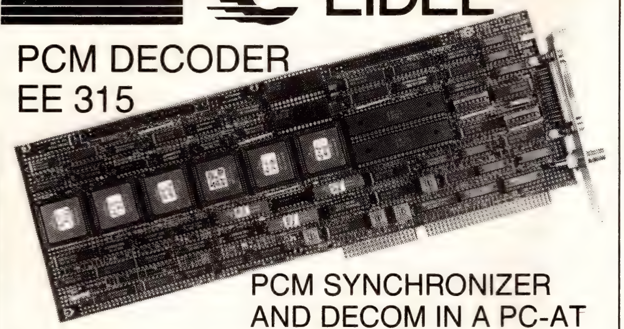

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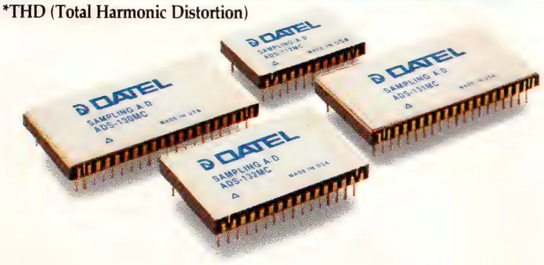

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properly, another circuit (a hand) reaches around and shuts off the start-up circuit. When the start-up circuit works properly, it saves power and doesn't waste much die area. Unfortunately, if the start-up circuit is broken or inoperative, the main circuit may still start if the supply voltage jumps up rapidly but may fail to start if the supply ramps up slowly. Once a customer returned a regulator complaining that the device would start if the supply ramped to 20V in 30 seconds, but not if it ramped in 36 seconds. We checked it out, and the customer was absolutely right. We had to change one mask and add a start-up test.

Sixteen years ago, an IC maker designed a micropower IC that didn't have a true dc start-up circuit. The IC was supposed to start up at the transient rise rate of the supply voltage. At room temperature, the circuit would always start, no matter how slowly the supply ramped up. But at cold temperatures, the device wouldn't start even with supplies of ±15V. Worse yet, if the device was running and you hit one of the power supply buses with certain positive or negative transients in sequence, you could turn the part OFF. Needless to say, that part never became popular, nor did anything else from that company.

So, let me caution you: Whether your circuit is a loop of sequential logic or an analog loop with positive and negative feedback, be sure to design it carefully. Add a test to make sure a bad part will be rejected, AND build up a few bad parts and make sure they fail the test. Then leave the test in the flow. Don't drop the test just because nobody has ever seen a part fail. Dropping that test would be courting disaster. Here at National Semiconductor, we've appointed a Czar of Start-up Circuits. He is the repository of all knowledge about circuits that do (and don't) start properly. Since this shy fellow (I shan't give his name) began to reign, the goof-up rate has been cut by many decibels. EDN

Author's biography

For information about Bob Pease, see the ***box,*** *"Who is Bob Pease, anyway?" on page 148 of the January 5, 1989, edition of EDN.*

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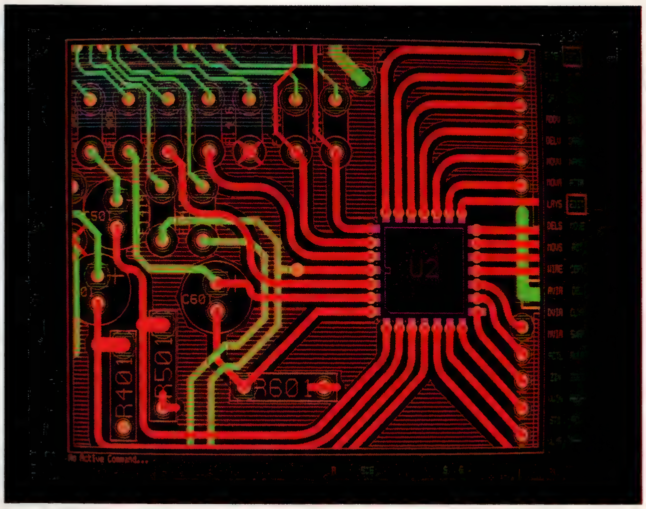

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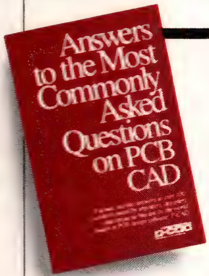

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CIRCLE NO 104

Interface power MOSFETs to logic devices

Though you can interface today's FETs directly to some logic devices, you must first evaluate such subtle points as low-supply-voltage conditions, power-supply on-off sequencing, and the reliability effects of the interface on the logic devices and the FETs.

Ken Berringer, *Semiconductor Products Sector, Motorola Inc*

Because of their fast switching speeds and low static losses, power MOSFETs are commonly used in switching applications. A power MOSFET turns on and has very low on-resistance when driven with sufficient gate voltage. If the gate voltage is insufficient to bias the power MOSFET fully on, or if the succeeding stage causes excessive drain currents, the power MOSFET will operate in the saturation (pinch-off) region. In other words, a certain gate voltage will support only a limited amount of drain current.

Most of the current crop of fourth-generation power MOSFETs require a gate drive of 10V to support their maximum continuous drain current; 5V logic won't provide enough voltage to drive a standard power MOSFET. However, a new family of logic-level power MOSFETs is available that can support their rated drain current with a gate voltage of 5V. With the proper considerations, you can interface these power MOSFETs to most logic families.

However, before you attempt to interface MOSFETs with standard logic, you must understand how gate drive, power losses, and switching speed affect your choices. A MOSFET's input capacitance, which is strongly affected by die size, influences its gate drive. Therefore, selecting the correct device for the application not only minimizes component cost, but also optimizes switching performance. A power MOSFET's on-resistance, $R_{DS(ON)}$, which is a function of junction temperature (T_j), gate voltage (V_{GS}), and drain current (I_D), determines static and dc losses. Vendors typically specify $R_{DS(ON)}$ at I_D equal to half the rated drain current, a V_{GS} of 10V, and junction temperatures of 25 and 100°C.

You can calculate the power MOSFET's static losses in dc or pulsed applications. First, using manufacturers' data-sheet curves, correct the rated $R_{DS(ON)}$ for your drain current and estimated operating temperature. Then multiply this value by the RMS load current squared $[P_{static}=(I_{RMS}2)\times(R_{DS(ON)}]$. Choose a power MOSFET with a current rating (I_D) and voltage rating (V_{DSS}) well above your worst-case load conditions. A good rule of thumb: Select a device with twice your worst-case RMS drain current and a voltage rating 25% above your worst-case drain voltage.

In high-frequency applications, switching losses are often more significant than static losses. To minimize them, you must decrease the switching times. When you use a power MOSFET in switching applications, *The gate-drive requirements of most power MOSFETs won't be satisfied by 5V logic.*

you can't model the gate as a simple capacitor because of the sizable displacement currents in the drain-to-gate capacitor, C_{rss}, brought on by large swings in drain-to-gate voltage. As a result, the total input capacitance, C_{iss}, varies greatly over the power MOSFET's operating range. You can use a piecewise-linear capacitor model for C_{iss} in order to find first-order approximations of switching times.

A better method of calculating switching times is to use gate-charge data from manufacturers' data sheets. Although designers usually think of power MOSFETs as voltage-controlled devices, these parts can be accurately modeled as charge-controlled devices. The charge required for a power MOSFET to handle a given current is relatively constant even though its drain-to-gate capacitance, C_{rss}, varies drastically with drain-to-gate voltage. The value of C_{rss} may increase 1000% or more over the operating range.

When a current source drives a power MOSFET, **(Fig 1a)**, its gate voltage will be nearly piecewise linear **(Fig 1b)**. The three distinct regions are turn-on delay, (t_0 to t_1), rise time, (t_1 to t_2), and excess-charge time, (t_2 to t_3). At the end of the turn-on delay the power MOSFET begins to conduct, but the drain current is still very small. During the rise time the power MOSFET actually turns on, and the drain voltage drops to almost zero. The resistive-switching rise time, t_{rise}, is the time it takes the drain voltage to drop from 90% of its highest value to 10%. Although you are measuring the voltage, the specification rise time refers to the drain-current rise time. The drain-current rise time is the time that V_{GS} remains in the plateau region of **Fig 1b**. During the excess-charge time, $R_{DS(ON)}$ continues to decrease. During turn-off, you must remove this excess charge; driving the gate to an unnecessarily high voltage will increase the total turn-off time.

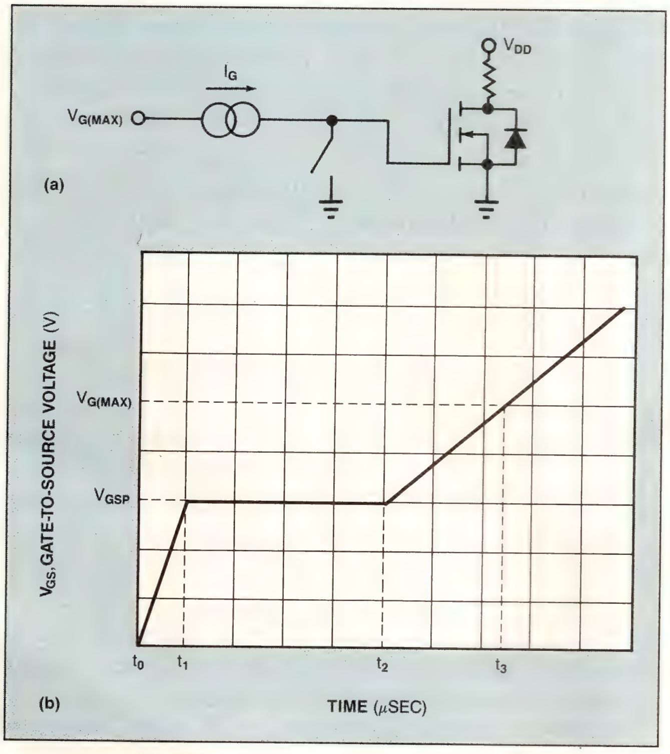

***Fig 1—If a constant current source, I_G, drives a power MOSFET* (1a)*, you can model the gate voltage of the MOSFET with a piecewise linear input model* (1b).**

Unlike bipolar transistors, power MOSFETs are majority-carrier devices. Without minority injection, you can turn power MOSFETs off and on with equal ease. For identical gate-drive currents, the rise time will equal the fall time. The turn-off waveform for a constant gate current will be a mirror image of **Fig 1b**. Note that the turn-off delay does not equal the turn-on delay; instead, it corresponds to the turn-on excess-charge time.

Since the gate current in **Fig 1b** is constant with and equal to the charge-per-unit time, you can label the horizontal axis "time" or "charge". Typically, you measure gate charge data by using a 1-mA current source; that is, it will provide 1 nC of charge in 1 msec. Manufacturers' data sheets usually include a gate-charge chart of V_{GS} vs Q_g, with Q_g measured in nanocoulombs **(Fig 2)**. It is important to note that the plateau voltage, which is the value of V_{GS} during rise time, increases with I_D. Therefore, the turn-on delay time also increases. Also, the amount of charge needed for rise time will vary with the drain-supply voltage. The gate-charge charts indicate this dependence by multiple lines for the excess-charge region as a function of V_{DS}.

To determine the switching times when using a current source to drive a power MOSFET, use the gate-charge chart to find the charge required to turn the MOSFET on, **(Fig 2)**, and then use the equation:

$$t=Q_g/I_G. \qquad (1)$$

Find the charge required during the turn-on delay region, $Q_{d(ON)}$, by drawing a line down from the first inflection point to the horizontal axis of **Fig 2**. The intersection of this line with the axis is the gate charge for the rated or tested I_D. If your actual drain current is different from the rated current, you may improve accuracy by linearly scaling $Q_{d(ON)}$. You can scale $Q_{d(ON)}$ by looking at the device's output-transfer curve, I_D vs V_{GS}, and by adjusting V_{GS} to yield the appropriate I_D. Then, calculate the turn-on delay by using **Eq 1**.

Next, use the gate-charge chart to find the gate charge required for rise time (Q_{rise}). The gate charge is the distance between the first inflection point and the intersection of the plateau with the line for your expected V_{DS}. A typical value is sometimes listed as Q_{gd}. You can use this value to calculate both rise and fall times. Then, find the intersection point of your maximum V_{GS} and the line corresponding to your V_{DS}. This intersection is the total gate charge, $Q_{g(TOTAL)}$.

To find the charge required for turn-off delay, $Q_{d(OFF)}$, subtract $Q_{d(ON)}$ and Q_{rise} from $Q_{g(TOTAL)}$. Manufacturers often specify a maximum total gate charge, $Q_{g(MAX)}$, to facilitate worst-case design. However, this figure sometimes includes a substantial guardband.

Thevenin sources complicate the calculations

When you're driving a power MOSFET with a voltage source and a series resistance (a Thevenin source), the calculations are more complex. During rise and fall times, V_{GS} is relatively constant, because all the gate current charges the gate-to-drain capacitor. By Ohm's law, I_G is also constant; you can use the gate-charge chart with **Eq 1** to find rise and fall times. During turn on, the voltage across the series resistance is the effective source voltage (usually the supply voltage) minus the gate-to-source plateau voltage, V_{GSP}. During turn off, the voltage across the resistor is the plateau voltage minus the effective sink voltage (usually ground). Rise and fall times will therefore typically be different. By using this information with **Eq 1**, we can obtain an equation for rise time:

$$t_{rise}=Q_g/I_G=(Q_{gd})(R_{eff(ON)})/(V_{SOURCE}-V_{GSP}), \qquad (2)$$

and fall time:

$$t_{fall}=Q_g/I_G=(Q_{gd})(R_{eff(OFF)})/(V_{GSP}-V_{SINK}). \qquad (3)$$

V_{GSP} is the power MOSFET's gate-to-source plateau voltage, V_{SOURCE} is the gate driver's effective source voltage, V_{SINK} is the gate driver's effective sink voltage, and R_{eff} is the gate driver's effective resistance (output resistance). During turn off, V_{SINK} may be near 0V or may even be a negative voltage.

Because gate current is not constant during turn-on and turn-off delays, you can't use gate-charge data to determine switching speeds. The series resistance and the gate capacitance form an RC network. However, the capacitance varies greatly over the operating range. To find the switching times, you must determine the capacitance for each region from a capacitance chart like the one in **Fig 3**. During the turn-on delay, V_{DS} is near its maximum value, V_{GS} is near zero, and the input capacitance is low. Find the value of C_{iss} in the capacitance curve for your maximum value of V_{DS} and use this capacitance, Point A in **Fig 3**, to calculate the

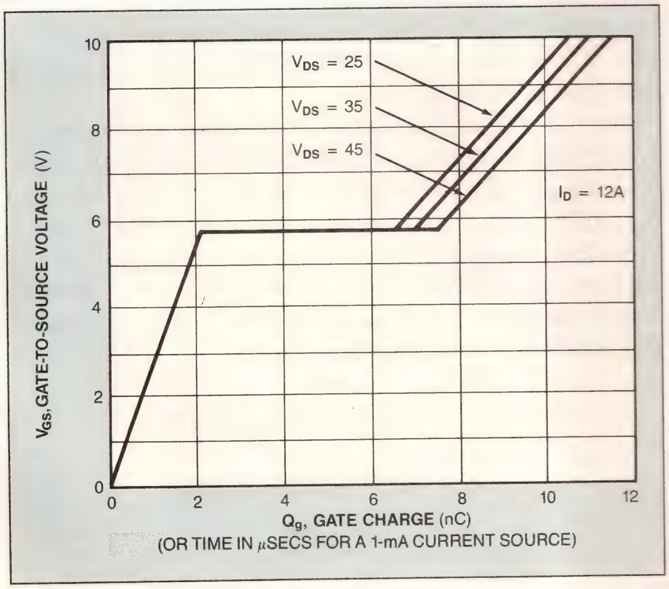

Fig 2—A gate-charge chart for a MOSFET *helps you calculate the switching times of the MOSFET being driven by a current source.*

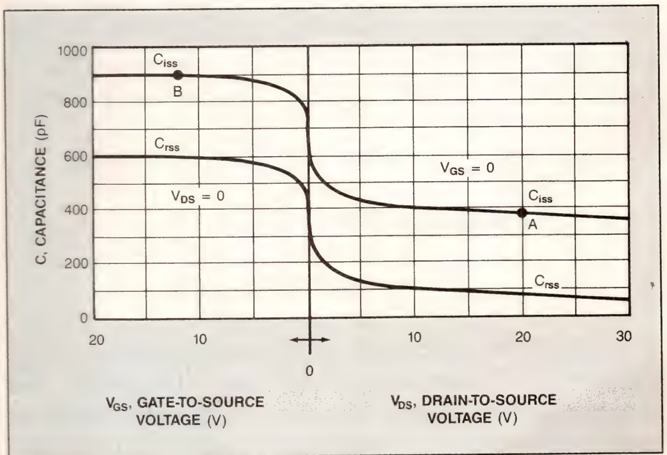

Fig 3—Capacitance charts are useful for switching speed calculations *because the capacitance of the MOSFET's gate varies with the gate voltage.*

Even though a MOSFET's drain-to-gate capacitance varies widely, the charge for a given current is relatively constant.

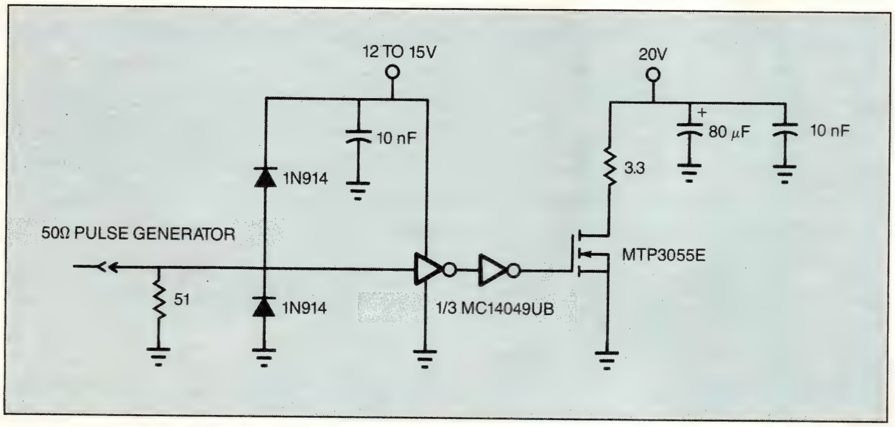

Fig 4—To compare calculated and measured switching times, *construct a simple CMOS interface circuit to drive a power MOSFET.*

turn-on delay. You can use the following equation to approximate the turn-on delay time:

$$t_{d(ON)}=(R_{eff(ON)})(C_{iss(MIN)}ln[(V_{SOURCE}/(V_{SOURCE}-V_{GSP})]. \quad (4)$$

During the turn-off delay, V_{DS} will be low and C_{iss} will be larger than the turn-on C_{iss}. Find the value of C_{iss} corresponding to $V_{DS}=MIN$ and $V_{GS}=MAX$ (Point B on the capacitance chart.) Then, to approximate turn-off delay time, use the equation:

$$t_{d(OFF)}=(R_{eff(OFF)})(C_{iss(MAX)})ln[(V_{G(MAX)}-V_{(SINK)})/(V_{GSP}-V_{SINK})], \quad (5)$$

$V_{G(MAX)}$ is the initial gate voltage prior to turn off (usually the supply voltage), $R_{eff(OFF)}$ is the effective series resistance during turn off, and V_{SINK} is the effective sink voltage. If V_{SINK} is at ground, the V_{SINK} terms will drop out of **Eq 5**.

Note the relationship between the gate-charge chart and the capacitance curves. The slope of the line in the gate-charge chart is in volts per nanocoulombs. A Farad of capacitance is equal to a coulomb per volt:

$$I(\text{coulomb/sec}) = (C)(dV/dt)(\text{Farad-volts/sec}).$$

From this equation, you find that

$$\text{Farad} = \text{coulomb/volt}.$$

Therefore, the reciprocal of the slope is the input capacitance in nanofarads (1000 pF). However, you should use both charts. The gate-charge chart is most useful when the input capacitance varies, and the gate current is constant during rise and fall times. The capacitance curve is most useful when the input capacitance is constant, and the gate current varies during delay times.

You can interface standard power MOSFETs directly to standard CMOS devices, such as the MC14000 family. This family uses complementary P- and N-channel FETs for the output stage. Although standard outputs are rated at ±10 mA and buffer outputs are rated at ±45 mA, saturation currents for short-circuit conditions are much higher. Although you should not short-circuit a CMOS gate for long periods of time, the gate may be safely operated in the saturation region when switching large capacitive loads. A 14049UB inverter buffer can typically source 30 mA and sink 120 mA, using a 12V supply. If you don't take steps to limit the output current, the CMOS gate's output will act like a current source. If you limit the output current to less than the saturation currents, the CMOS gate's output will act like a voltage source with a finite output resistance. The MC14000 series will operate from 3 to 18V. The common 12 or 15V V_{DD} supply will adequately drive power MOSFETs.

You can connect the 14049UB directly to a standard-power MOSFET such as the MTP3055E **(Fig 4)**, which is a rugged 12A, 60V power MOSFET. You have no output-series resistor to limit the gate-drive current; therefore, the gate-drive current will be equal to the 14049's output-saturation currents of +30/−120 mA. Using the gate-charge data with **Eq 1**, you can predict the following switching times:

$$t_{d(ON)}=2\text{ nC}/30\text{ mA}=67\text{ nsec};$$

$$t_{rise}=4\text{ nC}/30\text{ mA}=133\text{ nsec};$$

$$t_{d(OFF)}=6\text{ nC}/120\text{ mA}=50\text{ nsec};$$

$$t_{fall}=4\text{ nC}/120\text{ mA}=33\text{ nsec}.$$

TABLE 1—SWITCHING TIMES FOR STANDARD CMOS DEVICES DRIVING AN MTP3055E

DRIVER	V_{CC} (volts)	R_G (Ω)	$t_{d(on)}$ (nsec)	t_{rise} (nsec)	$t_{d(off)}$ (nsec)	t_{fall} (nsec)
4049UB	12	0	50	150	60	50
4049UB	12	220	60	300	200	150
4049UB	12	470	100	400	400	300
4049UB	15	0	40	100	70	40
4049UB	15	220	50	200	280	120
4049UB	15	470	75	330	500	420
4050B	12	0	50	150	60	50
4050B	12	220	60	300	200	150
4050B	12	470	100	400	400	300
4069UB	12	0	100	360	340	250
4069UB	12	220	115	500	380	370
4069UB	12	470	150	680	530	580
4069UB × 2	12	0	70	260	170	130

NOTES:
I_D = 6A UNLESS NOTED.
ONE GATE USED UNLESS NOTED.

The switching times are measured using the circuit in **Fig 4**; the measured switching times are shown in **Table 1**.

Considering that the circuit speed is high enough for the circuit to suffer from parasitic degradation, the calculated values are fairly accurate for first-order approximations. The 14049's saturation currents vary from device to device and with the supply voltage and the junction temperature. Driving directly from the logic IC will provide the quickest rise and fall times, but these times can vary by more than 50%.

By adding a resistor between the CMOS buffer's output and the gate of the power MOSFET in **Fig 4**, you can control switching times by limiting gate-drive current. However, adding or increasing the gate resistor also increases the power MOSFET's susceptibility to noise and accidental dv/dt turn on. A rapid change in the power MOSFET's drain voltage will cause a voltage to appear on the gate that may be sufficient to turn the gate on. Keeping the driver impedance low will minimize or eliminate this phenomenon.

To find the switching times while using a gate resistor, use **Eqs 2** and **3** to find rise and fall times. Then, use **Eqs 4** and **5** to find the delay times. Here, $R_{eff(ON/OFF)}$ equals the gate resistor, R_g, plus the CMOS-buffer's output resistance, R_o. The approximate output resistance of the 14049 is 200Ω for turn on and 50Ω for turn off. Let V_{SOURCE} equal V_{DD} and V_{SINK} equal zero. **Table 1** summarizes switching times for several gate resistors.

The letters UB in the MC14049UB stand for "unbuffered." Each path through the 14049 consists of a single inverter. The additional gate in **Fig 4** ensures that the power MOSFET driver is itself driven to V_{DD}. The input voltage will greatly affect saturation currents and, therefore, switching times. The MC14050B is a "buffered," noninverting buffer that consists of two cascaded inverters. Therefore, it does not invert the signal and is less susceptible to soft-drive conditions. The diodes on the input in **Fig 4** clamp the input voltage to ground and V_{DD}. Excessive voltage applied to a CMOS input may damage its internal static-protection diodes. Voltage applied to the output of a CMOS device that exceeds the supply voltage, V_{DD}, may cause the device to latch-up and destroy itself. Remember to decouple the logic device; it is drawing substantial currents.

You can also use open-collector TTL gates to drive standard-power MOSFETs. However, most open-collector output stages were designed for 5V operation. Low-power Schottky (LS) gates such as the 74LS05

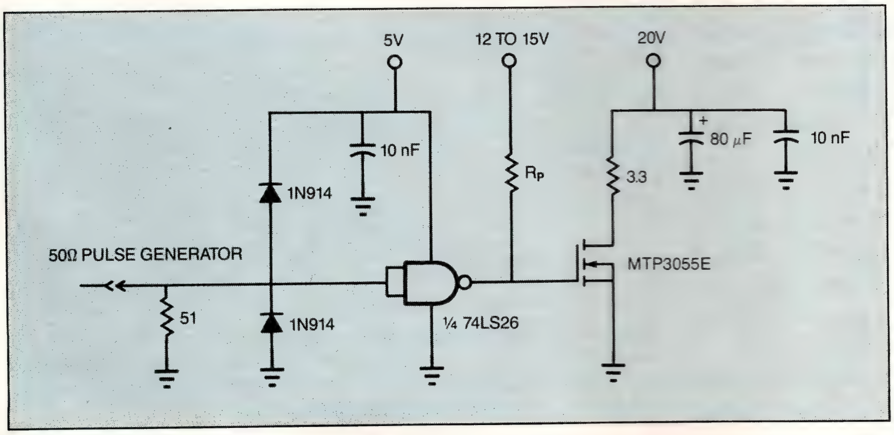

Fig 5—A 74LS26 quad NAND device interfaces with a power MOSFET. *Use a 1.5-kΩ pullup resistor to V_{CC} to limit the steady-state sink current to 8 mA; this action guarantees the logic device's V_{OL}.*

Thevenin sources complicate the calculations for turn-off delay.

typically have a collector-emitter breakdown voltage of 10 to 15V. The breakdown limitation makes them unsuitable for operation using a 12 or 15V supply. The TTL gates can be operated from an 8 to 10V supply or with an 8 to 10V zener clamp on the output. However, in these configurations, long-term reliability of the logic device will suffer.

The 74LS26 is unique among 74LS devices in that it interfaces to 15V logic and has a tested collecter-emitter breakdown greater than 15V. You can use this quad NAND gate to drive a power MOSFET with a single pullup resistor **(Fig 5)**. Using a 1.5k-Ω pullup resistor with a 12V supply will limit the steady-state sink current to 8 mA—a limitation that is necessary to guarantee the 74LS26's rated-output low voltage V_{OL} of 0.5V. Using a smaller pullup resistor would increase the device's V_{OL}, and consequently increase the drain-to-source leakage current of the power MOSFET in the off state.

During turn on, the pullup resistor supplies the current; during turn off, the 74LS26 must sink both the gate current and the pullup resistor current. The pulldown transistor of an LS output will typically sink about 30 mA. You calculate turn-on times using **Eqs** 2 and 4 with $R_{eff(ON)}=R_p$ and $V_{SOURCE}=V_P$, where R_p is the pullup resistor and V_P is its supply voltage.

To calculate turn-off times use **Eqs** 3 and 5, with $R_{eff(OFF)}=R_p$ and $V_{SINK}=V_p\text{-}I_{SINK}R_p$ (V_{SINK} may be negative). The equations for $R_{eff(OFF)}$ and V_{SINK} are the Thevenin equivalents of an ideal constant-current source working against a pullup resistor. The V_{SINK} equation is only valid when you approximate the pulldown transistor as a current source. During turn-off delay and fall times, the pulldown transistor provides a nearly constant sink current, since the pulldown transistor's collector-emitter voltage exceeds its $V_{CE(sat)}$ and the base-drive current is relatively constant.

The 74LS26 with a 1.5-kΩ pullup resistor drives the MTP3055E in **Fig 5**. The switching times are summarized in **Table** 2. The configuration shown in **Fig 5** provides minimum rise and fall times. However, fall times will vary greatly, since the 74LS26's sink current will vary with temperature and from device to device. A series-gate resistor can be used to slow and control turn off. You calculate switching times using **Eqs** 2 through 5. For gate resistors larger than 1 kΩ, use the following approximations: $R_{eff(ON)}=R_p+R_g$, $V_{SOURCE}=V_P$, $R_{eff(OFF)}=R_g$, and $V_{SINK}=0.5V$.

TABLE 2—SWITCHING TIMES FOR THE 74LS26 DRIVING AN MTP3055E

V_{CC} (volts)	R_G (Ω)	R_P (Ω)	$t_{d(on)}$ (nsec)	t_{rise} (nsec)	$t_{d(off)}$ (nsec)	t_{fall} (nsec)
12	0	1500	200	850	240	175
15	0	1800	200	750	300	175
12	1500	1500	450	2000	1300	1450
12	3000	3000	930	3900	2500	2900

NOTES:
I_D=6A UNLESS NOTED.
ONE GATE USED UNLESS NOTED.

You can easily interface logic-level power MOSFETs to 5V logic devices. These FETs have a larger transconductance and a lower threshold voltage than their conventional counterparts. More importantly, manufacturers specify $R_{DS(ON)}$ at $V_{GS}=5V$. Unfortunately, most 5V logic families don't have 5V high-output (V_{OH}) capability. Fast-Schottky (FAST) and low-power Schottky (LS) logic have a minimum rated V_{OH} of 2.7V, so you must use a pullup resistor to 5V in order to drive logic-level power MOSFETs. High-speed CMOS (HC) has a V_{OH} rating of 4.95V, and therefore does not need a pullup resistor.

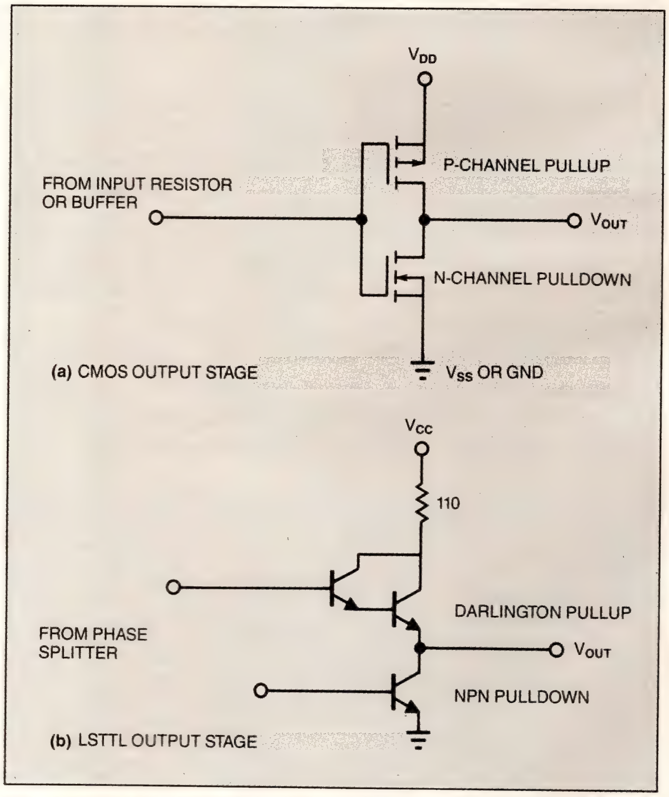

Fig 6—The CMOS-output stage* (6a) *is usually buffered from the internal logic and is optimized from the manufacturer to operate at 5V. The LS-output stage* (6b) *uses a totem-pole output and is current-limited on both pullup and pulldown to about 30 mA.

TABLE 3—SWITCHING TIMES FOR LOGIC DEVICES DRIVING A LOGIC-LEVEL MTP3055EL

DRIVER	R_P (Ω)	$t_{d(on)}$ (nsec)	t_{rise} (nsec)	$t_{d(off)}$ (nsec)	t_{fall} (nsec)	COMMENT
74HC04		25	120	85	75	
74LS04	560	45	450	120	130	
74F04	220	15	170	18	21	
74HC04		10	65	30	30	2 gates
74HC04		10	125	35	45	12A 50°C

NOTES:
I_D = 6A UNLESS NOTED.
ONE GATE USED UNLESS NOTED.

Fig 6 shows the output stages of HC- and LS-logic devices. The HC-output stage in **Fig 6a** is identical to the standard CMOS-output stage, save that the complementary MOSFETs have been optimized for 5V operation. Most HC devices are buffered by additional complementary stages. The LS-output stage in **Fig 6b** uses a totem-pole output. The pulldown transistor is biased on by about 500 μA and has a β of about 60, so it can sink a maximum of 30 mA. When the output is shorted, the 110-Ω resistor limits the pullup transistor's sink current to about 30 mA.

Figures 7a and **7b** show you how to interface HC, LS, and FAST logic to logic-level power MOSFETs. Note the input-termination and protection circuitry, which is external to the logic chip. This circuitry is necessary to drive the logic device with anything other than another logic device. It is best to drive the logic-level power-MOSFET driver with a device from the same logic family. When connecting an HC (or any CMOS) device to an off-board connector, the diodes should be used for ESD protection.

The measured switching speeds for the HC-, LS-, and FAST-logic families driving a logic-level power MOSFET **(Figs 7a)** and **(7b)**, are shown in **Table 3**.

You can connect a 74HC04 hex inverter directly to a logic-level power MOSFET. Perform the calculations for switching times the same way as for the CMOS inverter buffer. The 74HC04 will source and sink about 50 mA with a 5V supply.

The HC family's operating supply range is 2 to 6V. An HC device will drive a logic-level power-MOSFET gate to within 50 mV of V_{DD}. However, if the V_{DD} supply falls below 5V, the switching times and $R_{DS(ON)}$ will increase dramatically. If V_{DD} reduces 10%, to 4.5V, rise time increases by about 50%; fall time increases roughly 15%. $R_{DS(ON)}$ increases from 10 to 100% or more, depending on the drain current and the junction temperature. If low-voltage operation is a real possibility, you should choose a logic-level power MOSFET and a heat sink to handle this worst-case condition.

Data-sheet curves provide information

Examine the curves for "On-region Characteristics," "$R_{DS(ON)}$ vs ID," and "$R_{DS(ON)}$ vs Temperature" in manufacturers' data sheets. You may need to use a device with a current rating much larger than your expected load current to attain the desired $R_{DS(ON)}$ under low-supply conditions. Manufacturers are now developing 4V logic-level power MOSFETs with $R_{DS(ON)}$ rated at 4V. You can interface these devices to HC-logic devices and operate them down to 4V levels. However, the lower threshold voltage makes the devices more susceptible to noise and increases leakage currents.

The 74LS04 in **Fig 7b** must have a pullup resistor to 5V. A minimum pullup resistor of 560Ω guarantees the logic device's output-low-voltage, V_{OL}, of 0.5V. During turn on, gate-drive current is supplied by the pullup resistor and the 74LS04's internal pullup transistor. During turn off, the 74LS04 must sink both the gate-drive current and the pullup resistor current. A larger R_p will increase turn-on time and decrease turn-off time. A smaller R_p would increase the V_{OL} of the 74LS04, increasing the power MOSFET's leakage current. The lower threshold voltage of logic-level power MOSFETs makes the V_{OL} rating critical. The threshold voltage of a power MOSFET decreases as temperature increases. Therefore, the V_{OL} of the logic device must be less than the logic-level power MOSFET's threshold voltage $V_{GS(th)}$ at its maximum expected junction temperature. For this reason 4V logic-level power MOSFETs may be incompatible with TTL-logic devices.

Switching times can again be estimated by using the Thevenin equivalents of the drive circuit with **Eqs 2** through **5**. During turn-on delay, the 74LS04's Darlington pullup transistor and the external pullup resistor supply current. The Darlington is in saturation with a $V_{CE(sat)}$ of about 1.5V. The 110-Ω pullup resistor limits the 74LS04's output current. To calculate turn-on delay time, you could use **Eq 4** with $V_{SOURCE} = V_{CC}-[1.5R_p/(R_p + 110\Omega)]$ and $R_{eff(ON)} = R_p$ in parallel with 110Ω. During rise time, the pullup resistor supplies nearly all the current, since V_{GSP} is usually above the 74LS04's V_{OH}. You may therefore use **Eq 2** with $V_{SOURCE} = V_{CC}$ and $R_{eff(ON)} = R_p$ to estimate rise time.

During turn off the pulldown transistor must sink the gate current and the pullup resistor current. To

Don't short-circuit a CMOS gate for long periods of time. However, you may operate it in the saturation region when switching large capacitive loads.

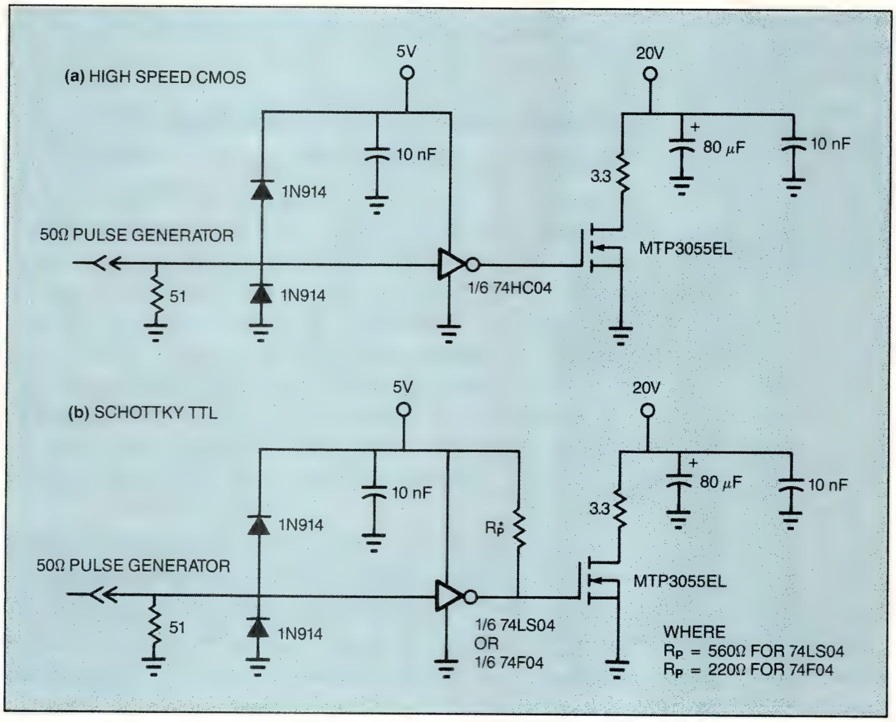

Fig 7—These circuits show some simple ways to drive logic-level power MOSFETs. *HC logic can drive these MOSFETs without a pullup resistor* **(7a)** *whereas both LS and FAST logic require a pullup resistor* **(7b)**.

calculate turn-off times, use $V_{SINK} = V_{CC}-(I_{SINK})(R_p)$ and $R_{eff(OFF)} = R_p$ with **Eqs** 3 and 5. The pulldown transistor's maximum sink current, I_{SINK}, is typically about 30 mA.

The 74LS family's specified supply-voltage range is from 4.75 to 5.25V. The rise time of the MOSFET's gate input will vary greatly with supply voltage while the fall time varies only by about 5%. Because the supply voltage affects both the pullup resistor current and the pullup transistor current, rise time will vary from about +80% to -40% for V_{CC} equal to 4.75 and 5.25V, respectively. Since the operating supply range of LS logic is less than that of HC logic, $R_{DS(ON)}$ will not vary as much, but must be considered.

FAST handles higher currents

The FAST logic family can source and sink much more current than the LS family. The 74F04 can source about 50 mA and sink about 200 mA. A minimum pullup resistor of 220Ω will guarantee the logic-device's output-low voltage V_{OL} of 0.5V. A larger R_p will increase turn-on time and decrease turn-off time. You can calculate switching times for the FAST family the same way you do for the LS family. To limit the pullup Darlington's output current, the 74F04 uses an internal 35Ω resistor instead of the 110Ω external resistor. The same supply-voltage considerations for the LS family apply to the FAST family.

You can use a series gate resistor with either of the circuits in **Fig 7** to slow and control switching times. With $R_{eff(ON/OFF)} = R_g$ and **Eqs 2** through **5**, you can estimate the switching times for large gate resistors (greater than 200Ω for HC, 5 kΩ for LS, and 2 kΩ for FAST). When switching loads are even slightly inductive, the inductive kick-back during turn off may cause the drain voltage to rise above the load supply. Slowing down the turn off with a gate resistor will reduce this voltage. If this kick-back voltage is large enough and contains sufficient energy, it may destroy the power MOSFET. A family of rugged power MOSFETs can handle considerable energy under these conditions.

You may also want to choose a large R_g value in order to reduce EMI. When driving a lamp, you may want to use a very large resistor to limit in-rush current. Using a gate resistor and/or a larger pullup resistor will also improve the long-term reliability of the logic device. The gate resistor, not the logic device, dissipates most of the gate-drive power losses, thereby reducing stress on the logic-output devices. A larger pullup resistor limits the steady-state on-current in the pulldown transistors, thereby decreasing their power dissipation. However, using a large gate resistor increases the power MOSFET's susceptibility to noise and dv/dt turn on.

Given enough time, the TMS320C25 can do almost everything the ADSP-2100 can.

The ADSP-2100.

- The ADSP-2100 computes a 1024-point complex FFT in less than 3 ms with a total memory requirement of less than 4k bytes. It also computes a 2 × 2 2D convolution in 1.2 μs and executes ADPCM in only 68 μs.
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- The ADSP-2100 supports zero-overhead loops of any length. So our looped code – which is the easiest to write – is also the fastest.
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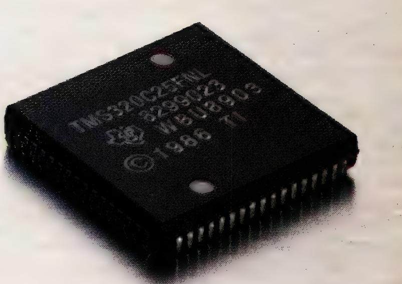

The TMS320C25.

- The TMS320C25 takes more than three times as long to compute the same size FFT, while it devours over 47k bytes of memory.[1]
- The TMS320C25 is limited to one access of external data every two cycles.
- The only zero-overhead loop the TMS320C25 can execute is one instruction repeated no more than 256 times.
- Circular buffers? The TMS320C25 doesn't support them.
- The TMS320C25 is programmed with 133 mnemonics like SPAC, BGEZ, MACD, XORX, and SBRK. A multiplication/accumulation is coded as MACD >FF03,*–. While this might not scare the XORX out of you, it's not the easiest thing to debug or maintain.

We're not saying the TMS320C25 is slow. But even if it were twice as efficient as it is now, it'd still be a lot slower at DSP than the ADSP-2100. The fact is, the ADSP-2100 is out in front of the TMS320C25 in performance, readability of code, and development tools.

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[1] EDN, "EDN's DSP Benchmarks," September 29, 1988.

The 14049UB has unbuffered inverting outputs; the 14050B has buffered noninverting outputs.

Although you can use series-gate resistors to slow switching speeds, you can achieve faster switching by connecting like logic gates on the same chip. The output-current capability increases in proportion to the number of paralleled gates you use. If you don't use a gate resistor, the switching times decrease in proportion to the number of paralleled gates. If you do use a gate resistor, you may safely decrease its value, in proportion to the number of gates, to decrease switching times. Paralleling logic gates will not appreciably change the total logic-package power dissipation, because the output current increases and switching times decrease. When you use many gates, switching times may decrease to the point where the times are limited by the stray inductance in the load and in the layout. You should not parallel logic gates on different chips or from different families because the different propagation delays may cause excessive shoot-through currents, which might damage the logic devices.

High currents can cause supply noise

You can also use spare gates left over from a digital circuit to drive a logic-level power MOSFET. However, the large currents used by the driver may cause large amounts of noise on the supply rail. This noise may cause data errors in the other gates on the same IC. Limiting the current with a large gate resistor and carefully decoupling the logic device will reduce the power-supply noise. Also, to avoid ground-shift problems caused by the large drain currents, you should ground the driving logic device at the same point as the source of the power MOSFET. If you use separate logic and analog grounds, connect them only at the source of the power MOSFET.

Pay close attention to the power-supply scheme. Never leave the gate of a power MOSFET floating while a voltage is applied to the drain. If you do, and you don't limit the drain current, the power MOSFET could turn on and destroy itself. If you use separate supplies for the load and the logic IC, the logic supply should be powered up first and powered down last. If this is not possible, consider what happens to the logic-device output when power is removed. The pullup resistors in the LS and FAST circuits of **Fig 7b** will pull the power MOSFET's gate down to V_{CC} when V_{CC} is low, turning the power MOSFET off. The HC inverter's output, however, will be in a high impedance state when the logic-supply voltage is low, allowing the power MOSFET's gate to float. Using a large resistor to the logic-supply voltage or ground, or using a small signal diode to clamp the output below the logic-supply voltage, will solve this potential floating-gate problem.

Low logic-supply voltage may also cause power MOSFET failure due to insufficient gate drive. When a power MOSFET fails, the drain voltage will usually appear at the FET's gate and may blow out the entire logic circuit. A gate resistor will also limit the current under this power MOSFET failure condition.

You can also interface μPs to a power MOSFET using either of the circuits in **Fig 7** as a buffer between a μP's port and a logic-level power MOSFET. If you want to use a standard power MOSFET, you will have to use the 74LS26 circuit in **Fig 5** or a level shifter. You can use the MC14504B hex level shifter to interface HC, LS, or FAST logic to standard CMOS. This level shifter can either drive the power MOSFET directly or it can work with a buffer like the MC14049UB in **Fig 4** to decrease switching times. The MC14504B has selectable TTL/CMOS-level inputs and standard CMOS outputs. It can source and sink a maximum of about 20 mA using a 12V supply.

Be very careful when using bus drivers and latches that have 3-state outputs, like the 74LS240/74HC240 and 74LS373/74HC373, to drive a power MOSFET. The LS 3-state devices require a pullup resistor to drive the power MOSFET to 5V, and as a result will leave the power MOSFET on when the outputs are disabled. The HC devices with 3-state outputs, in contrast, will let the FET gate float when its own outputs are disabled, possibly damaging the power MOSFET. You can only use 3-state devices if you tie the output enable pin low for negative-logic enable inputs. HC 3-state devices do not require a pullup resistor to drive a logic-level power MOSFET, and may therefore be used with a pulldown resistor to ground. Note that you should never allow a 3-state output on a logic device to be pulled above the supply rail or below ground.

μCs can drive a MOSFET

When simplicity is important, you can use a single-chip μC like the 68HC11 to directly drive a power MOSFET. The 68HC11 performs such functions as pulse-width modulation (PWM) and complex motor-speed control; it can also control multiple-power MOSFETs for bridge applications. When you use the μC in its single-chip mode, any one of the 8 pins of parallel output-port B can drive a logic-level power MOSFET. Unfortunately, if you use a large, gate-

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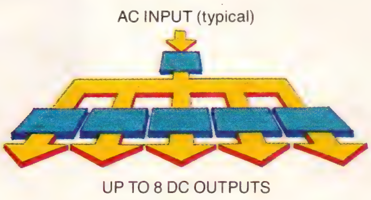

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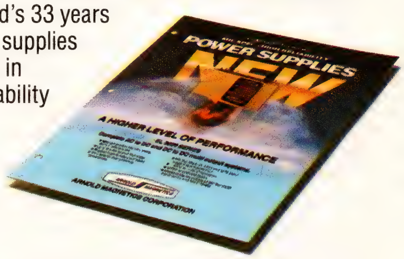

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To accelerate switching times, parallel like devices on the same logic device; conversely, slow switching by adding a series gate resistor to the MOSFET.

series resistor to minimize power dissipation and noise on the chip, your switching times will be fairly slow. This arrangement also exposes the µP to possible harm from power-MOSFET failure. Although all the outputs of port B will be reset to zero by a Power-On Reset (POR), using a pull-down to ground ensures that the power MOSFET will be off during power-down. In some applications, it may be necessary to initialize the power MOSFET gate drive via software before you supply power to the power MOSFET.

You can also use port B in a strobed mode by using the STRB signal from control port D. The STRB signal will go high after the data on port B is valid and may be used to latch or enable a logic device driving a power MOSFET. This mode may be useful when you want exact synchronization between the µC-controlled devices.

When you use the µP in the extended-memory mode, ports B and C are used for address and data buses. The 68HC24 port-replacement unit can replace port B in a software transparent fashion. Thus, you can develop a system using the 68HC11 with a 68HC24 and external memory, while the final product will use only the 68HC11.

These examples show that you can interface standard-power MOSFETs directly to standard CMOS logic without significant performance impact—about 50-nsec rise and fall times for the MC14049UB driving a 12A power MOSFET. Another alternative is to interface standard power MOSFETs to 5V logic using an interface device such as the 74LS26 open-collector NAND gate or the MC14504B hex level shifter. The 74LS26 driving a 12A standard-power MOSFET gives turn-on times of about 1 msec and turn-off times of less than 200 nsec. Further, you can estimate switching times using **Eqs 2** through **5** and, by selecting the appropriate output-series resistor, you can tweak the driver to give the desired rise and fall times of the power MOSFET.

Whereas HC logic can directly drive logic-level power MOSFETs, LS logic requires the addition of a pullup resistor. You can realize switching speeds of less than 150 nsec per gate when driving a 12A power MOSFET with HC logic. Using an LS device to drive the power MOSFET, turn-on speed is good—about 0.5 msec; turn-off speed is excellent—less than 150 nsec. Again, you can estimate switching speeds and select a series resistor to give the performance you want.

Logic power-supply variations are the most important aspect affecting logic-level power MOSFET performance. Power-supply sequencing and undervoltage protection is necessary to ensure system integrity. And don't ignore circuit layout and power-supply decoupling at high speeds. Finally, you can interface a logic-level power MOSFET directly to a dedicated µP-output port when you want µP control.

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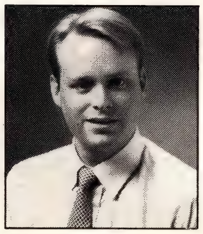
Author's biography

Ken Berringer is a power-applications engineer with Motorola's Semiconductor Products Sector, where he develops R&D applications using power MOSFETs and bipolar transistors. Ken earned his BSEE at the University of Florida. In his spare time, he enjoys golf and playing guitar.



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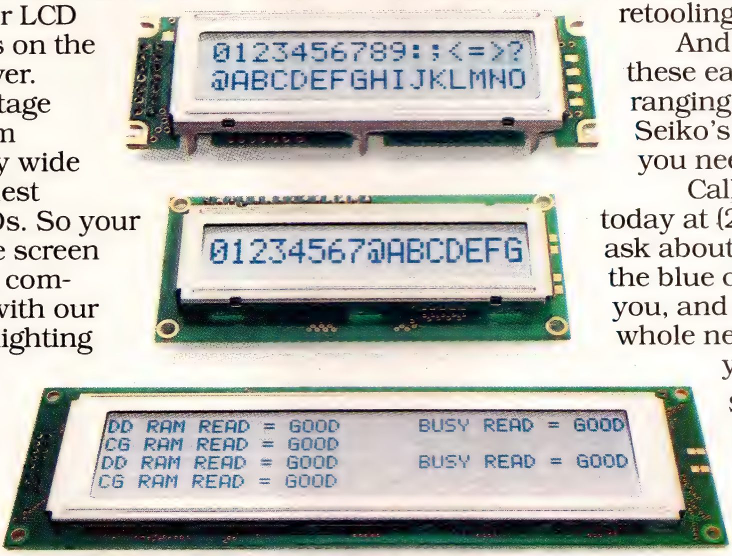

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DSP µP extracts mean and variance

Yosi Gabayan
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The TMS320C10 DSP µP program in **Listing 1** calculates the mean and variance of a set of input samples. The program uses the formulas:

$$V_{DC} = \frac{\{X(1) + \ldots + X(n)\}}{n}$$

$$V^2 = \frac{\{X(1) \times X(1) + \ldots + X(n) \times X(n)\}}{n}$$

$$VAR = V^2 - V_{DC}^2.$$

The program works with a sample rate of 8k samples/sec, and for the sample set, n is 256 8-bit samples. The program was designed for measuring the performance of telephone equipment.

To Vote For This Design, Circle No 748

LISTING 1—MEAN AND VARIANCE DSP PROGRAM

```
***** INITIALIZE VARIABLES *****************************
      ZAC
      SACL  DCL      INITIALIZE DC VOLT LOW BYTE
      SACL  DCH      INITIALIZE DC VOLT HIGH BYTE
      SACL  ACL      INITIALIZE AC VOLT LOW BYTE
      SACL  ACH      INITIALIZE AC VOLT HIGH BYTE
      LACK  1
      SACL  ONE
      LAC   ONE,8
      SACL  T256     COUNTER FOR 256 MS
***** TAKE SAMPLES FOR 256 MS *************************
      LAC   T256,3
      SACL  COUNT
F3    CALL  INPUT     READ SAMPLE
*.... CALCULATE THE MEAN .............................*
      ZALS DCL
      ADDH DCH
      ADD  SAMPLE
      SACL DCL
      SACH DCH        DC = DC + SAMPLE
*.... CALCULATE SECOND MOMENT ........................*
      LT   SAMPLE
      ZALS ACL
      ADDH ACH
      MPY  SAMPLE
      APAC
      SACL ACL
      SACH ACH        AC**2 = AC**2 + SAMPLE*SAMPLE
*.... MEASURE TIME ..................................*
      LAC  COUNT
      SUB  ONE
      SACL COUNT      COUNTER = COUNTER - 1
      BGZ  F3
```

Table continued on pg 206

LISTING 1—MEAN AND VARIANCE DSP PROGRAM—continued

```
***** CALCULATE AC VOLTAGE AND DC VOLT **************
*.... AC**2 = | AC**2 -  DC**2/2**11 | /2**11 ......*
      ZALS DCL
      ADDH DCH
      CALL SQUARE    ACC = DC**DC/2**11
      SACH DCH       SAVE DC VOLT
      SUBS ACL
      SUBH ACH
      ABS
      CALL NORM11   DIVIDE BY 2**11
      SACL ACL
      SACH ACH
*.... AC VOLTAGE = (AC**2)**0.5 ....................*
      ZAC
      SUB  ONE
      SACL LOC0
ROOT  LAC  LOC0
      ADD  ONE
      SACL LOC0
      ZALS ACL
      ADDH ACH
      LT   LOC0
      MPY  LOC0
      SPAC
      BGZ  ROOT
      RET
******************************************************
```

Emulator replaces system ROM

Sudhi Cheepchol
Thai International Airways, Bangkok, Thailand

To debug ROM-based code, you can switch the address space of the memory emulator in **Fig 1** between two blocks of addresses: from 0000_{HEX} through $3FFF_{HEX}$ to 4000_{HEX} through $7FFF_{HEX}$. Thus, you can plug the emulator into your target or development system, set the emulator to the high bank, and download code to it as though it were RAM. By virtue of its built-in battery backup, you can unplug the emulator from your development system and replug it into your target system without losing any data. Subsequently, you switch the emulator to the low bank and run your downloaded code as though it resided in ROM.

To disable writing to the emulator during periods when the emulator operates as a ROM, you can introduce a manual switch into the chip-select line or add an extra qualifying line from your system under development.

The 6264LP-15 Hitachi CMOS static RAMs in the emulator draw less than 0.1 mA in standby mode. In the event you unplug the emulator, its power-shutdown circuitry (Q_1, Q_2, and associated components) puts the RAMs in standby mode. The emulator runs off its backup battery until you plug it back in to a powered system.

You can expand this design to a 16k-byte emulator by substituting larger HM6264-15 RAMs, and by using address line A_{13} and its complement to select between the two RAM chips. Naturally, plugging in a 74ALS00 in place of the MC14011 will allow the emulator to run faster at the expense of higher current consumption. EDN

To Vote For This Design, Circle No 746

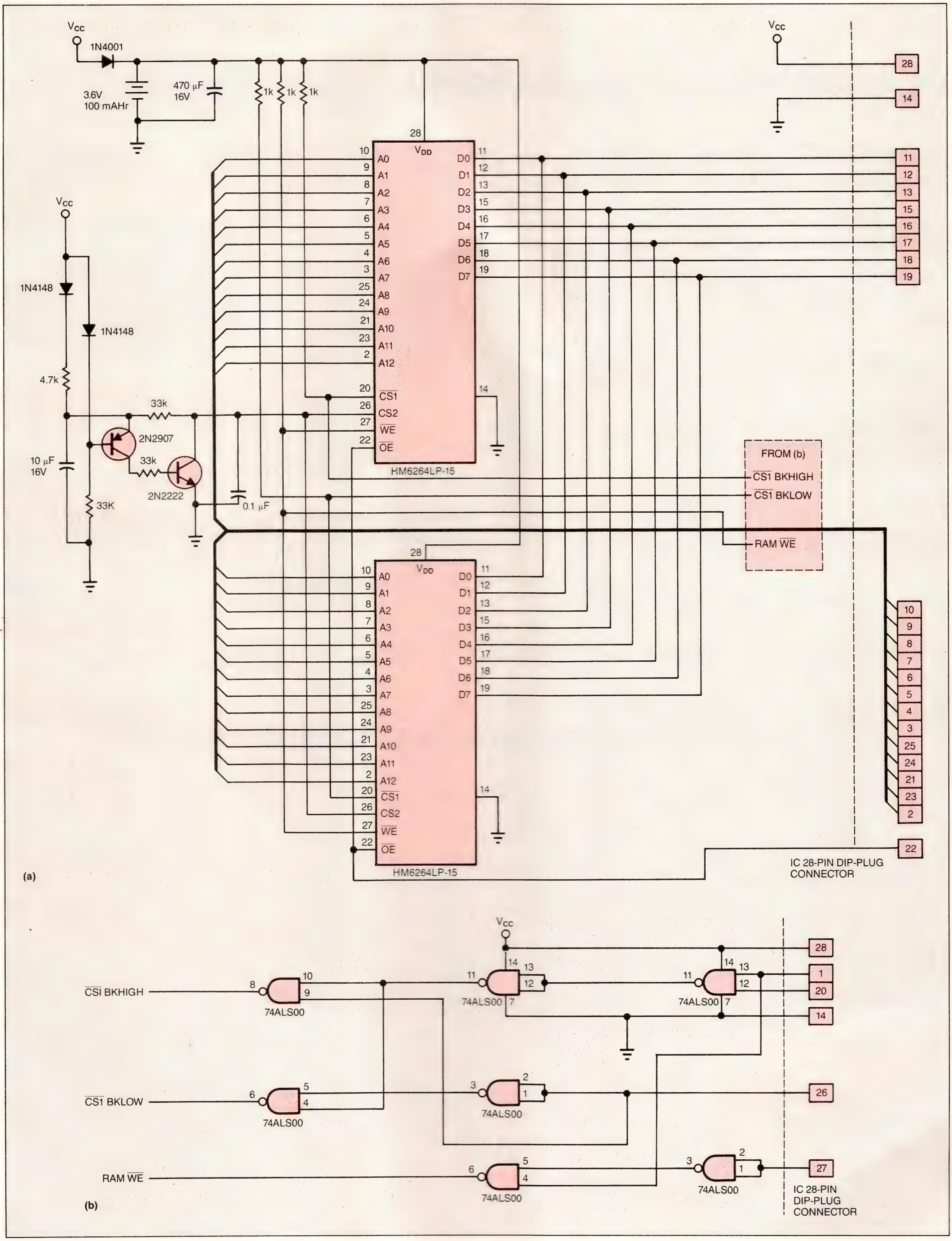

Fig 1—Because this ROM emulator has *a built-in backup battery, you can plug and unplug it at will from your target system.*

Spreadsheet computes frequency response

Joseph D Neglia and Doug Havenhill
Honeywell Satellite Systems, Phoenix, AZ

The spreadsheet program in **Listing 1** provides a simple means for calculating and graphing the gain and phase relationships of a transfer function. The program assumes that your transfer function is of the standard form:

$$G(s) = \frac{b_0s^5 + b_1s^4 + b_2s^3 + b_3s^2 + b_4s + b_5}{a_0s^5 + a_1s^4 + a_2s^3 + a_3s^2 + a_4s + a_5}.$$

The program in **Listing 1** has been set up according to this particular transfer function:

$$G(s) = \frac{1}{1 + 0.2s + s^2}.$$

The spreadsheet program uses the formula

$$|G(s)| = 20 \log \left[\frac{\sqrt{re\{N\}^2 + im\{N\}^2}}{\sqrt{re\{D\}^2 + im\{D\}^2}}\right]$$

in line I12 to calculate the gain of the transfer function, and

$$\phi(s) = \frac{180}{\pi}\left[\arctan\left(\frac{im\{N\}}{re\{N\}}\right) - \arctan\left(\frac{im\{D\}}{re\{D\}}\right)\right]$$

in line J12 to calculate the phase angle of the transfer function, where N is the numerator of the transfer function and D is the denominator. Because the numerator and the denominator can both be as complex as fifth-order functions, the formulas in lines E12 through H12 calculate their imaginary and real parts with these formulas:

$$re\{N\} = b_5 - b_3\omega^2 + b_1\omega^4$$
$$im\{N\} = b_4\omega - b_2\omega^3 + b_0\omega^5$$
$$re\{D\} = a_5 - a_3\omega^2 + a_1\omega^4$$
$$im\{D\} = a_4\omega - a_2\omega^3 + a_0\omega^5,$$

where ω is the frequency in radians per second.

You can easily extend this program for higher-order systems by expanding these expressions for the numerator and denominator. EDN

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LISTING 1—FREQUENCY-RESPONSE SPREADSHEET PROGRAM

```
A1: [W1] 'Frequency Response Program
A3: [W1] 'starting freq:
D3: [W6] 0.05
A4: [W1] 'points/decade:
D4: [W6] 50
A5: [W1] 'coefficients
D5: [W6] "s^0
E5: [W9] "s^1
F5: [W9] "s^2
G5: [W9] "s^3
H5: [W9] "s^4
I5: [W5] "s^5
A6: [W1] '  numerator:
D6: [W6] 1
E6: [W9] 0
F6: [W9] 0
G6: [W9] 0
H6: [W9] 0
I6: [W5] 0
A7: [W1] '  denominator:
D7: [W6] 1
E7: [W9] 0.2
F7: [W9] 1
G7: [W9] 0
H7: [W9] 0
I7: [W5] 0
B9: [W9] ^freq
C9: [W9] ^w
I9: [W5] ^Gain
J9: [W5] ^Phase
B10: [W9] ^(Hz)
C10: [W9] ^(rad/s)
D10: [W6] ^log(w)
E10: [W9] ^re{N}
F10: [W9] ^im{N}
G10: [W9] ^re{D}
H10: [W9] ^im{D}
I10: [W5] ^(dB)
J10: [W5] ^(deg)
B12: (S1) [W9] +D3
C12: (S1) [W9] +B12*2*@PI
D12: (F1) [W6] @LOG(C12)
E12: (S1) [W9] +$D$6-$F$6*C12^2+$H$6*C12^4
F12: (S1) [W9] +$E$6*C12-$G$6*C12^3+$I$6*C12^5
G12: (S1) [W9] +$D$7-$F$7*C12^2+$H$7*C12^4
H12: (S1) [W9] +$E$7*C12-$G$7*C12^3+$I$7*C12^5
I12: (F0) [W5] 20*@LOG(@SQRT(E12^2+F12^2)/@SQRT(G12^2+H12^2))
J12: (F0) [W5] 180/@PI*(@ATAN2(E12,F12)-@ATAN2(G12,H12))
                    .
                    .
                    .
```

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CIRCLE NO 108

Design Entry Blank

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DESIGN IDEAS

FEEDBACK AND AMPLIFICATION

New transformers update breaker

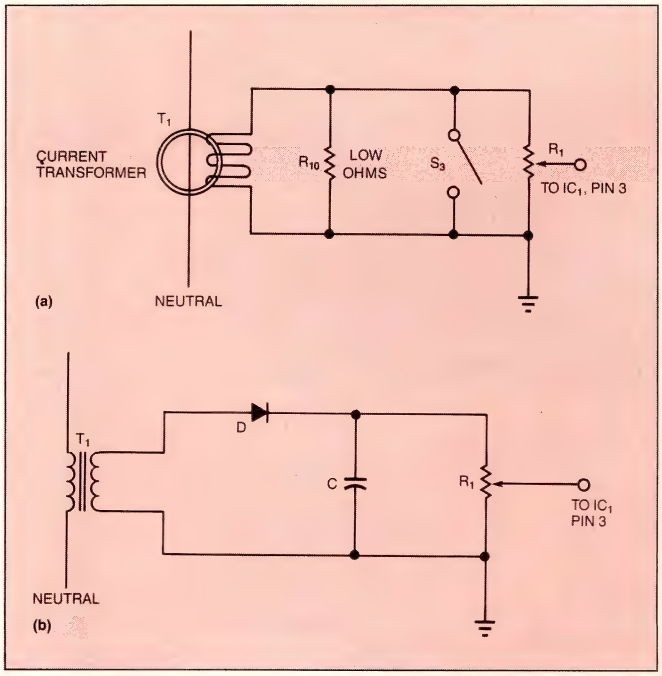
My original design for a sensitive electronic circuit breaker, "AC circuit breaker has adjustable threshold" (EDN, June 12, 1986, pg 211), used a nonstandard toroidal transformer. If you were to substitute a standard current transformer in my circuit, you could possibly generate excessive secondary currents or even blow the transformer up.

Unlike my original circuit, the circuit in the accompanying **figure** employs a standard current transformer in its usual shorted-secondary configuration. This circuit can safely handle the transformer's $5A^+$ secondary current.

You must select values for S_3, R_1, and R_2 to suit your current transformer. If you wish to improvise, you can modify a 120V/12V ac transformer to work in this circuit by adding a couple of turns to the transformer for the load current. Then you use the former primary winding as the secondary winding for the circuit in **Fig 1b**.

No matter which circuit you use, you should adjust R_1 to yield $-0.7V$ max at the connection to IC_1, pin 3.

Kurt French
NANVAL Corp
31 Roderick Rd
West Islip, NY 11795



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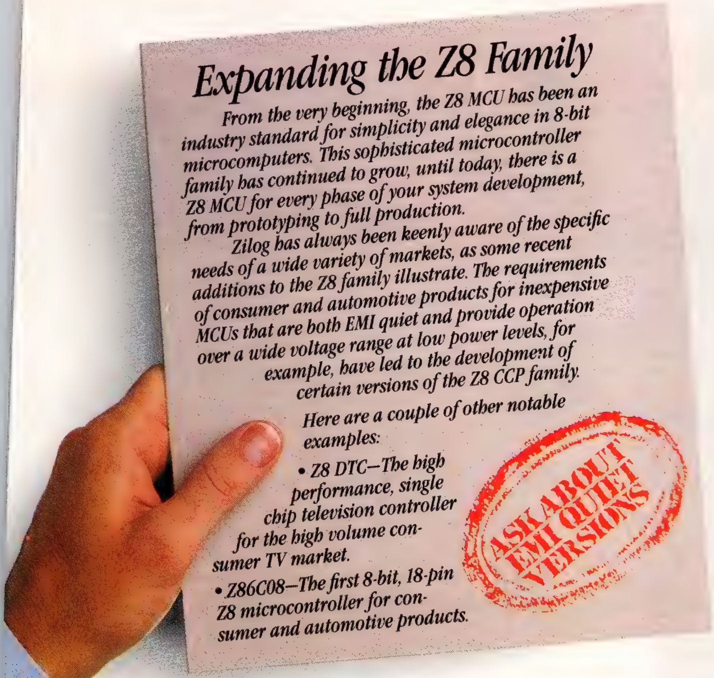

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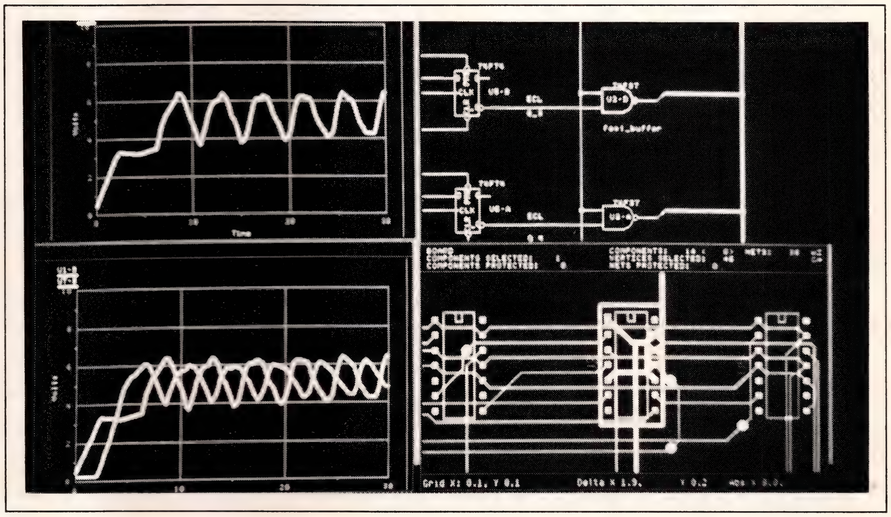

Swiftlogic Ltd, Badenheath Pl, Cumbernauld, Glasgow G68 9HX, Scotland. Phone 44 236 720748. FAX 44 236 730983.

Circle No 351

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- *Lets you run MS-DOS from ROM*
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- *Computes system production from component statistics*

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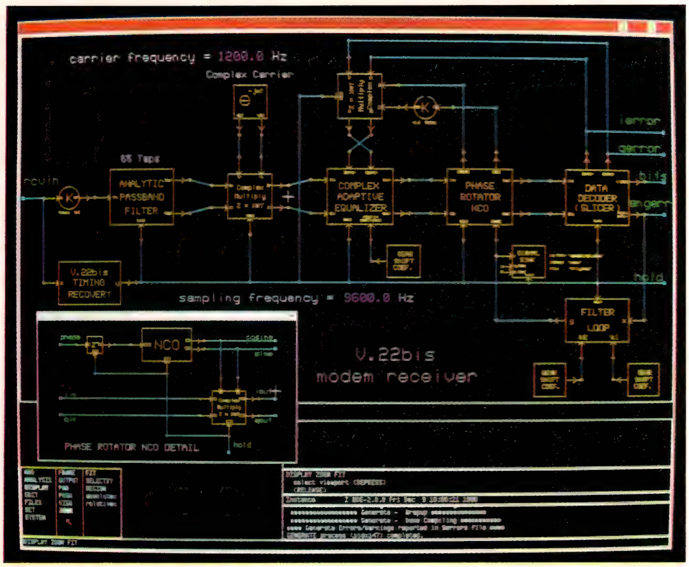

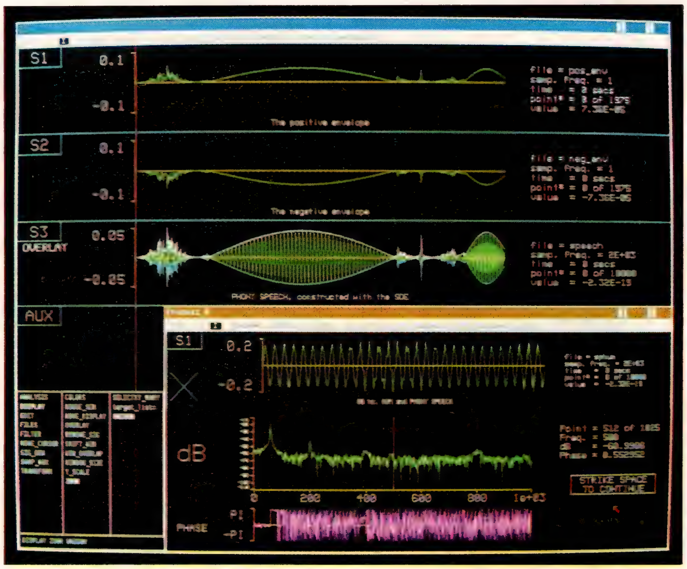

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Intermetrics, 733 Concord Ave, Cambridge, MA 02138. Phone (617) 661-1840. TWX 710-320-7523.

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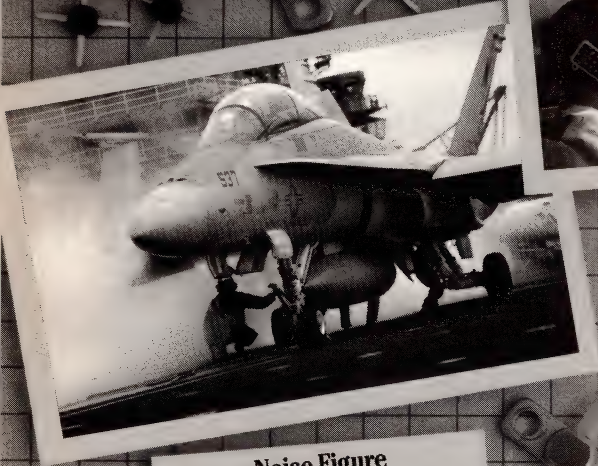
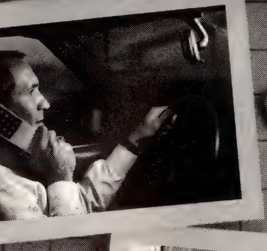

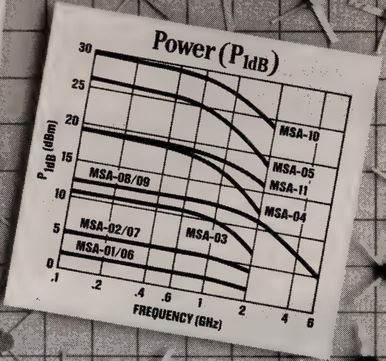

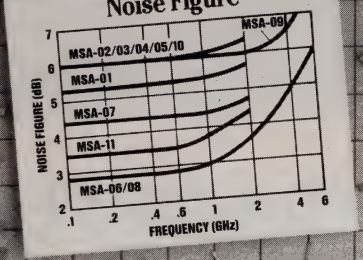

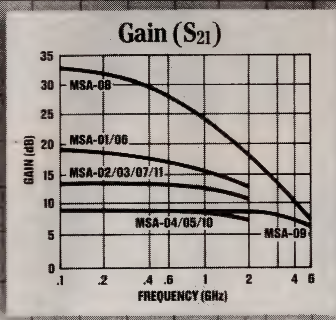

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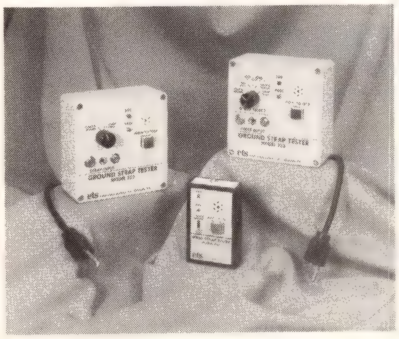

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- *Available in portable, wall-mount, and military versions*
- *Test strap resistance against high and low limits*

Models 250, 252, and 253 are testers for ground straps used to limit the electrostatic potential on people who work with static-sensitive components and assemblies. The 250 is portable and battery powered and provides an automatic low-battery indication. The 252 is intended for wall or pedestal mounting and is ac powered. Model 253 is a militarized unit that tests ordinance-type ground straps in addition to those used for grounding personnel. The units test straps against a low limit of 750 kΩ ±2% and a high limit of 1.25 MΩ ±2%. They test a strap plus the person wearing it against a high limit of 10 MΩ ±10%. The latter test assures that a strap is making good contact with the wearer. The 250, 252, and 253 are $100, $225, and $275, respectively.

Electro-Tech Systems Inc, 115 E Glenside Ave, Glenside, PA 19038. Phone (215) 887-2196. FAX 215-887-0131.

Circle No 359

80186 ANALYZER POD

- *Traces circuit activity at full speed*
- *Works with 80186, 80188, and CMOS equivalents*

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INTEL MICROCOMPUTER REFERENCE BOOKS

i860 64-BIT MICROPROCESSOR PROGRAMMER'S REFERENCE MANUAL
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i486 MICROPROCESSOR
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intel
386™ Microprocessor Hardware Reference Manual
intel
Microprocessor and Peripheral Handbook
Volume II—Peripheral
intel
Microprocessor and Peripheral Handbook
Volume I—Microprocessor

i860™ PROGRAMMER'S REFERENCE MANUAL

The Intel i860™ microprocessor delivers supercomputer-level performance using RISC design techniques in a single VLSI component. This manual provides the complete source of information needed by software designers and programmers. Included is an architectural overview and a complete description of the instruction set with programming examples.

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The i486™ CPU is 100% binary compatible with the 386™ CPU. One million transistors integrate cache memory, floating point hardware and memory management on-chip while retaining binary compatibility with previous performance levels. Some of the topics included in the book's thirteen chapters are: Real Mode Architecture, On-Chip Cache, Hardware Interface and Instruction Set Summary.

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386™ PROGRAMMER'S REFERENCE MANUAL

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386™ MICROPROCESSOR HARDWARE REFERENCE MANUAL

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8086/8088 USER'S MANUAL: PROGRAMMER'S AND HARDWARE REFERENCE

This completely revised and reorganized manual is divided into two sections. Section One, "Programming," is a general introduction. It contains an overview of information on the operation of the CPUs in the 8086/8088 family and gives some general design information. This section also includes a general description of the programming design of the 8087 Numeric Processor Extensions (NPX). Section Two, "Hardware," is a reference source. It contains specific hardware design information on the operation of the CPU's in the 8086/8088 family. This section also includes specific hardware design information on the operation and functions of the 8087 NPX.

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- *Adds ability to test µPs and LSI devices*

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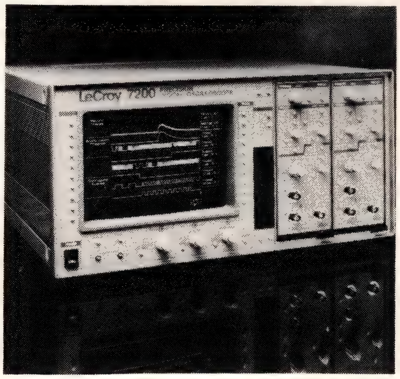
- *Can have four 8-bit inputs*
- *Have 400-MHz analog bandwidth*



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- *Will support 50- to 60-MHz μPs when they become available*

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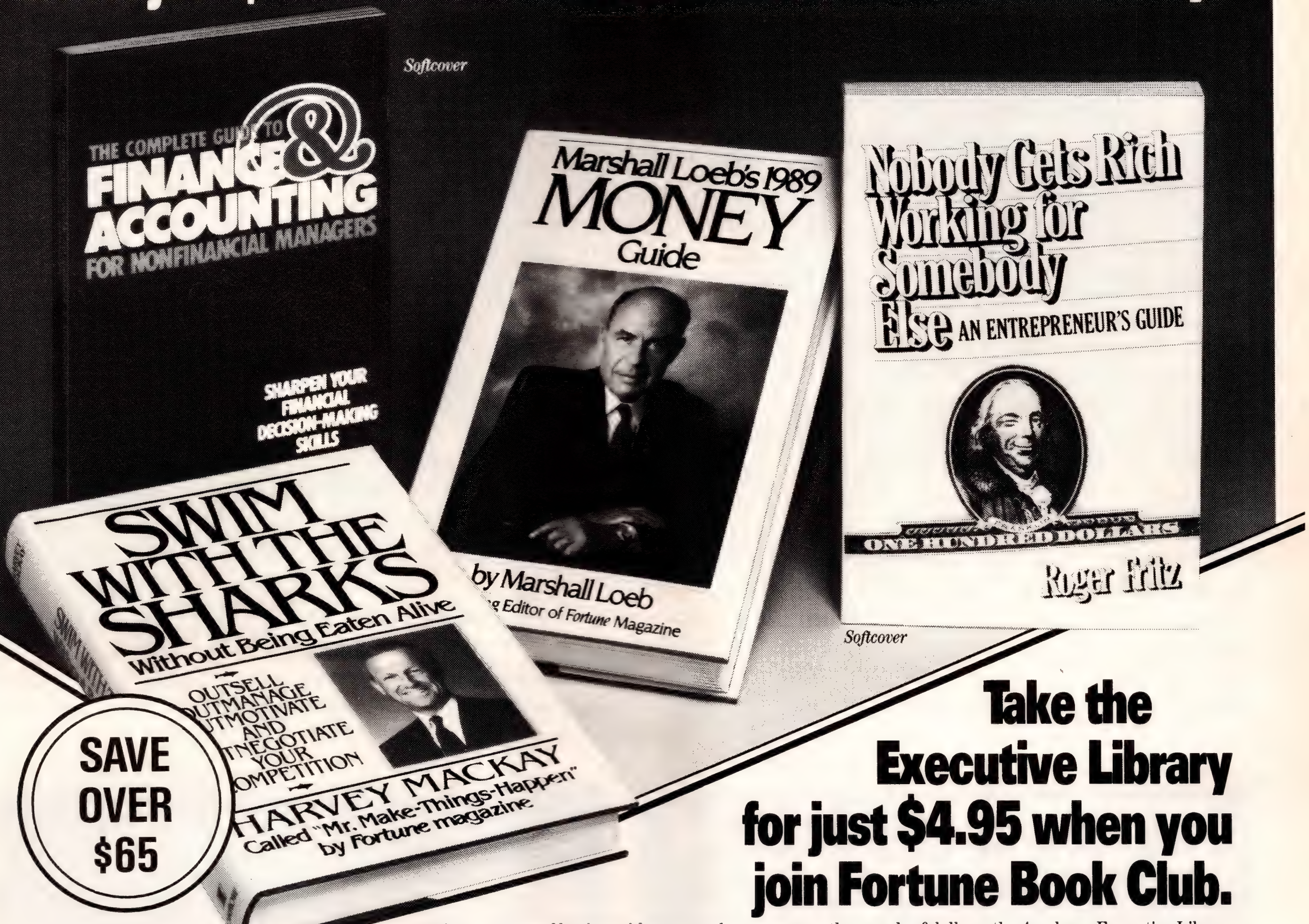

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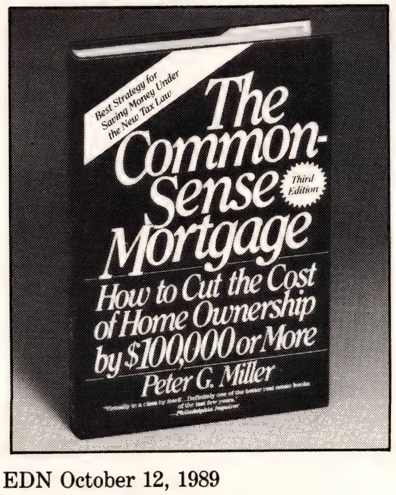

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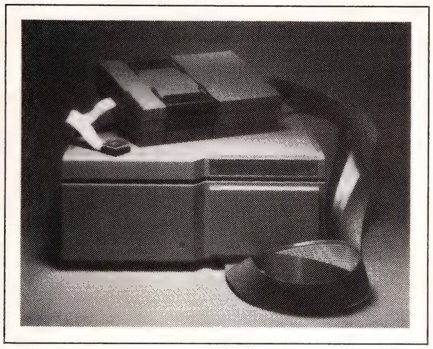


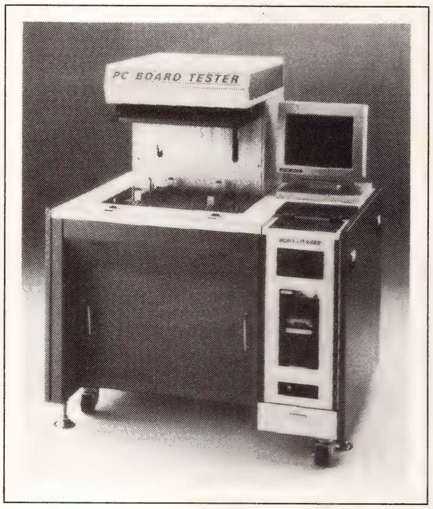
them. The emulator acts as a node on a network consisting of IBM PC-compatible computers or Sun workstations. You can access the in-circuit emulator from any other node, obviating a dedicated host. The emulator can break program execution on either instruction execution or access to specified memory addresses. The number of access breakpoints is limited only by the size of overlay memory—currently 2M bytes max. For debugging recursive routines, each of the six hardware execution breakpoints has a 32-bit real-time counter. The trace memory is 16k 139-bit frames. You can view captured trace data in real time without slowing the target µP. The vendor supplies a source-level debugging package and a window-based cross-development package. For 68020, $22,000; for 68030, $26,000. Prices include 512k bytes of overlay memory.

Applied Microsystems Corp, Box 97002, Redmond, WA 98073. Phone (800) 426-3925; in WA, (206) 882-2000. FAX 206-883-3049.

Circle No 364

IN-CIRCUIT TESTER

- *Can have 1024 test nodes*
- *Handles 2-sided probing of surface-mount boards*



The Model 510ZII in-circuit tester has 320 nodes. You can expand this number to 1024 nodes in increments of 64. The pneumatic-ram-operated fixture is suited to conventional boards and to 2-sided probing of boards containing surface-mounted devices. The system cancels stray capacitance and contact resistance and makes quadrature measurements. You can add optional boards to enable the tester to perform digi-

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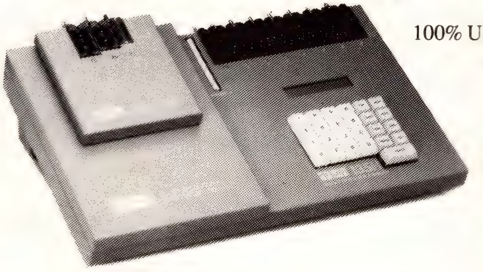

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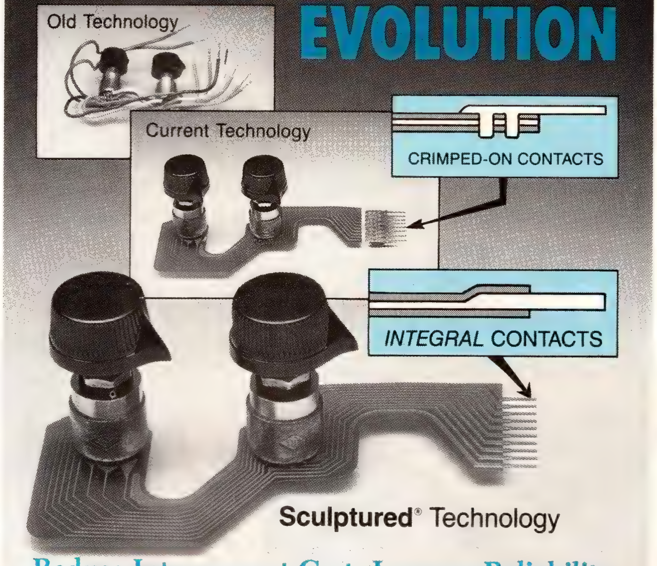

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Circle No 365

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- *Complies with IEC 801-4 for fast transients and bursts*

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- *Have a 16-level gray-scaling capability*
- *Available with back lighting*

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Hitachi America Ltd, Electron Tube Div, 300 N Martingale Rd, Schaumburg, IL 60173. Phone (312) 517-1144. FAX 312-517-1155.

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- *Features a 2-mW output*
- *Lases at 670 nm*

The SF 92 laser diode emits a narrow bright-red beam that allows you to confirm beam focusing with the human eye. The unit produces a 2-mW CW (constant wave) power output, has a lasing wavelength of 670 nm, and has operating and monitor current levels of 85 mA and 0.45 mA, respectively. Output beam diameter equals 2 mm. The diode measures 1×0.75×0.62 in. and can be modulated directly. $700.

Micro Laser Systems, 12771 Western Ave, Garden Grove, CA 92641. Phone (714) 898-6001. FAX 714-897-0979.

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TRANSDUCERS

- *Offer ±0.5% accuracy*
- *Measure gauge, sealed gauge, and absolute pressures*

Models 114 and 115 media-compatible pressure transducers measure from 5 to 5000 psi with ±0.5% accuracy. These solid-state units use 316 stainless-steel housing to protect the sensor from corrosive liquids and gases. The units are available in gauge ranges from 5 to 300 psi and sealed-gauge or absolute

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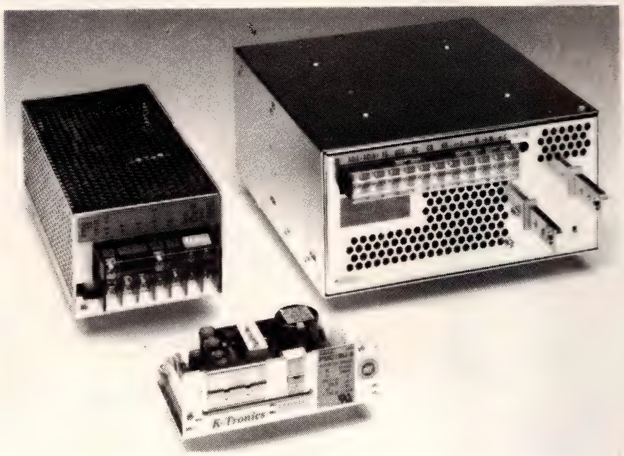

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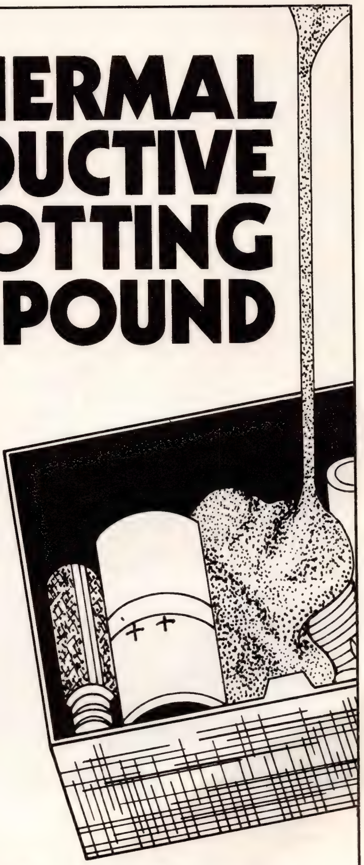

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IC Sensors Inc, 1701 McCarthy Blvd, Milpitas, CA 95035. Phone (408) 432-1800.

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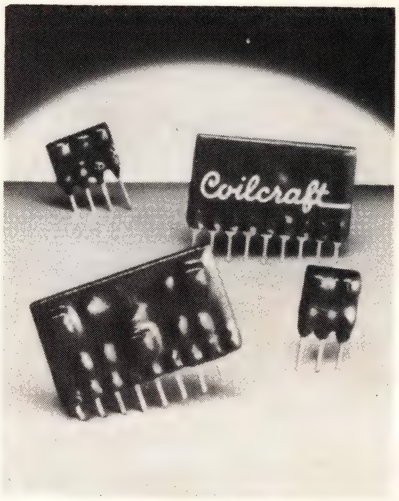


LC FILTERS

- *Have 0.5-dB max insertion loss*
- *Designed for LAN applications*

Units in this family of lowpass LC filters are designed for LAN adapter boards used in 10BaseT unshielded twisted-pair networks. The filters are available in 3-, 5-, and 7-pole versions in both balanced and unbalanced configurations. Passband impedances of 50 and 100Ω are available. Insertion loss is <0.5 dB to 10 MHz, and cutoff frequency equals 18 MHz. The 7-pole model provides 50-dB attenuation of frequencies from 30 to 200 MHz. Attenuation for the 5- and 3-pole versions equals 40 and 30 dB, respectively. The filters are housed in a SIP, which measures 0.6 in. for balanced designs and 0.5 in. for unbalanced versions. 7-pole, 50Ω filter, $2 (OEM qty).

Coilcraft, 1102 Silver Lake Rd, Cary, IL 60013. Phone (312) 639-6400.

Circle No 380

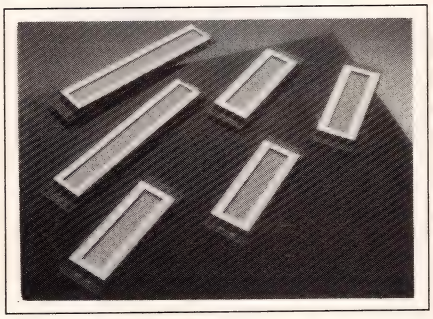
STEPPER MOTORS

- *Designed for high-torque applications*
- *Available in a choice of coil voltages*

Measuring only one inch in diameter, these stepper motors are designed for high-torque applications. The 7.5° version has a rated holding torque of 1.6 oz-in. with bipolar coils. The 15° version has a holding torque of 1.1 oz-in. with bipolar coils. Both motors are available with 5 or 12V coils as standard. Unipolar windings are also available. $5.30 (500). Delivery, stock to eight weeks ARO.

Haydon Switch & Instrument Inc, Box 3329, Waterbury, CT 06705. Phone (800) 243-2715; in CT and outside US, (203) 756-7441.

Circle No 381



LCD MODULES

- *Have an integral controller*
- *Display as many as 40 characters*

The modules in the LTN221R/F-10 family come assembled on a pc board and operate from a 5V supply. Available models will display two rows of 20 (221R/F-10), 24 (222R/F-10), and 40 (242R/F-10) 5×7 dot-matrix characters. Each type comes in reflective and transflective versions; the transflective models can have optional green backlighting. All the modules have an integral controller with a 160-character ROM and an 8-character RAM for user-definable symbols. The controller accepts 4- or 8-bit parallel data and has an extensive instruction set that includes display clear, cursor home, display on/off, cursor on/off, character blink, cursor shift, and display shift. The modules consume a maximum of 11 mW. Gld 28 to gld 50 (1000).

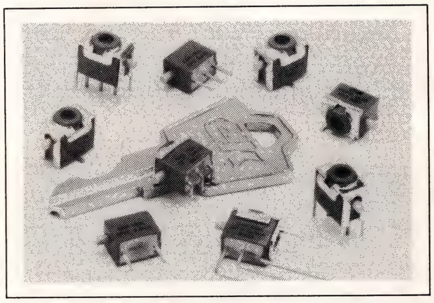
Philips Components, Box 218, 56 MD Eindhoven, The Netherlands. Phone 011-31-40-756181.

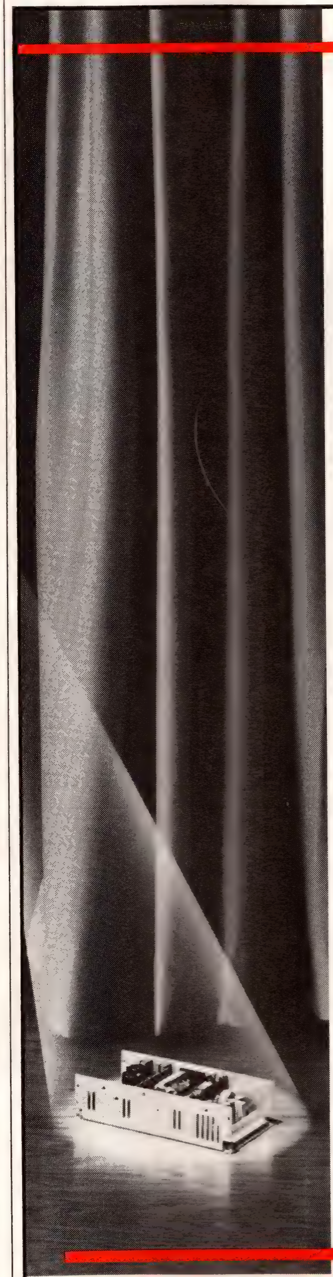
Circle No 382

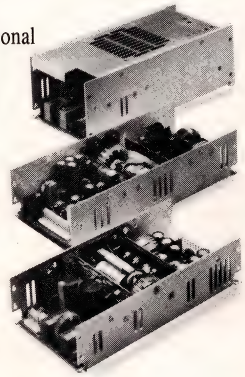
SEALED SWITCHES

- *Available in surface-mount and through-hole styles*
- *Offer a choice of contact configurations*

GP Series sealed pushbutton switches are available in both surface-mount and through-hole terminal styles. They are designed to







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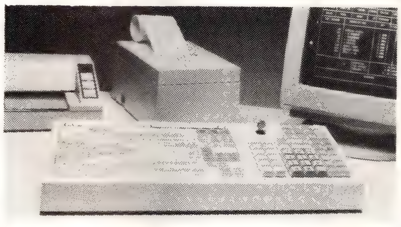
CIRCLE NO 130

withstand all soldering processes. Features include thermoplastic housings with a 94V-0 UL rating and internal O-ring actuator seals. The switches are available in spst and spdt versions. Straight, right-angle, and support-bracket terminal styles are offered with either 0.1- or 0.05-in. terminal spacings. Tin-lead terminal plating is standard. From $1.90 (1000).

C&K Components Inc, 15 Riverdale Ave, Newton, MA 02158. Phone (617) 964-6400.

Circle No 383



LAN KEYBOARD

- *Emulates a computer keyboard*
- *Can operate as a stand-alone unit*

Employing user-friendly point-of-sale software, the ECR/PC keyboard emulates a computer keyboard. Currently running on Novell and compatible networks, the unit interfaces with Arcnet or Ethernet communications protocol and uses diskless-workstation technology. The keyboard can communicate with as many as 255 workstations on the network via the host computer. The unit contains its own 8088-type CPU and has a RAM capacity of as much as 768k bytes. It has 58 full-travel keys and 140 flat-key positions. The keyboard is offered in both stand-alone and LAN versions. The stand-alone version includes RS-232C and IBM keyboard outputs. $585 to $1595.

Electronic Systems International, 23012 Del Lago Dr, Laguna Hills, CA 92653. Phone (714) 770-3246.

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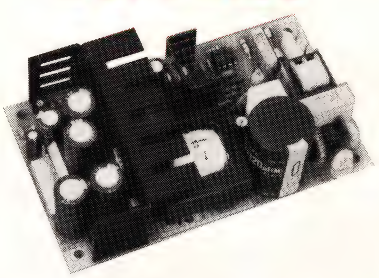
UNIVERSAL INPUT VOLTAGE SWITCHING POWER SUPPLIES



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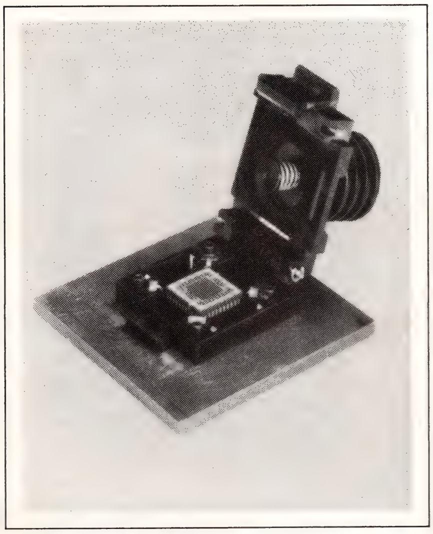

TEST SOCKET

- *Has an integral heat sink*
- *Features a 94V-0 UL rating*

The Cin'Apse chip-carrier test socket is designed for use with JEDEC-style leaded or leadless devices. It features a solderless interconnect, which allows testing of high-speed devices without introducing signal aberrations. The socket has a rated life of 25,000 mates/unmates and is designed to function over a −55 to +125°C range. The socket design features an integral aluminum heat sink, and the thermoplastic housing carries a 94V-0 UL rating. The termination scheme employs gold-plated, beryllium-copper button contacts. Electrical specs include a 4A current rating and 10-mΩ max contact resistance. $50 (1000). Delivery, eight to 10 weeks ARO.

Cinch Connector Div, 1501 Morse Ave, Elk Grove Village, IL 60007. Phone (312) 981-6000.

Circle No 385

POWER SUPPLIES

- *Offer IEEE-488 bus capability*
- *Output from 100 to 1000W*

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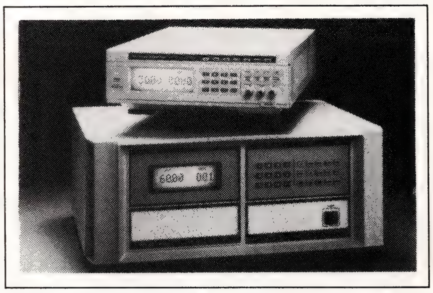

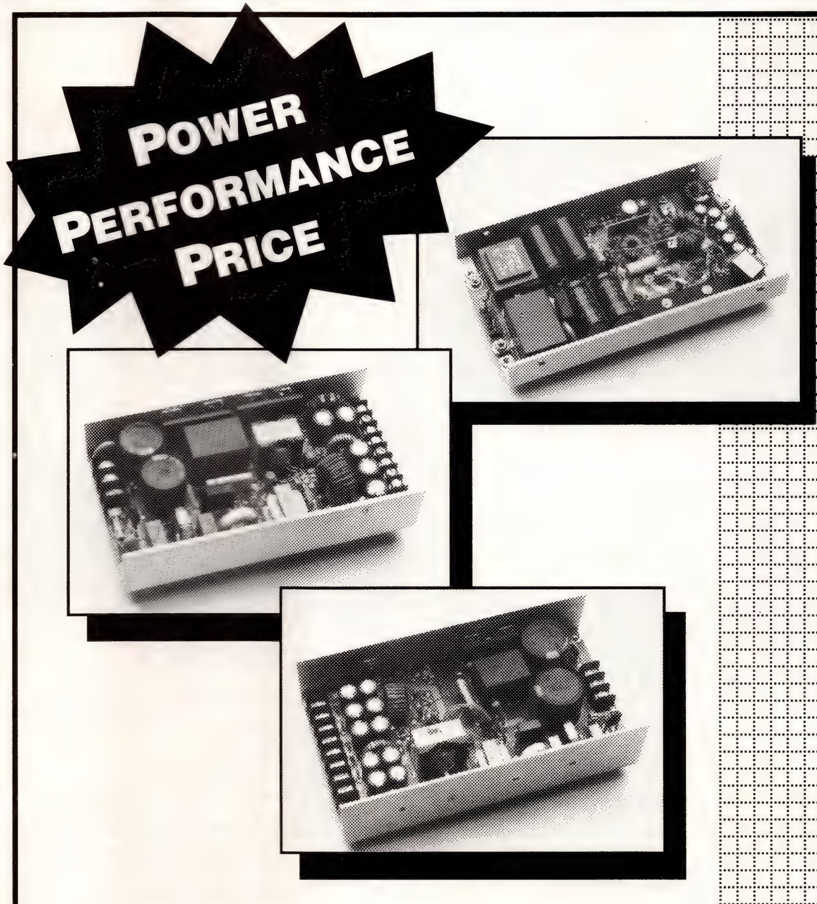

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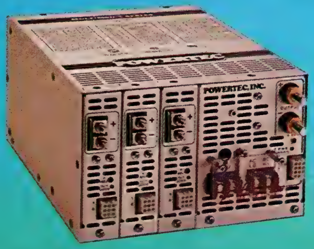

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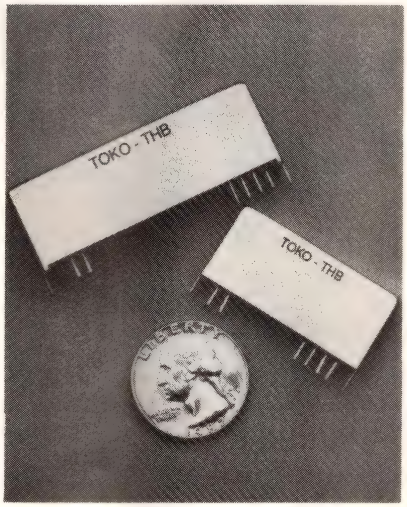

ACTIVE FILTERS

- *Available in bandpass and lowpass designs*
- *Feature SIP housing*

THB Series active filters are available in both bandpass and lowpass versions. Housed in a SIP, they use an operational amplifier to eliminate the need for any inductors. The bandpass units have a passband of 300 to 3000 Hz, and the lowpass models are available with cutoff frequencies of either 3, 14, 18, 20, or 22 kHz. Stopband attenuation is in excess of 30 dB for the bandpass filters and >36 dB for the lowpass types. $6 to $12 (500). Delivery, 12 weeks ARO.

Toko America Inc, 1250 Feehanville Dr, Mount Prospect, IL 60056. Phone (312) 297-0070. FAX 312-699-7864.

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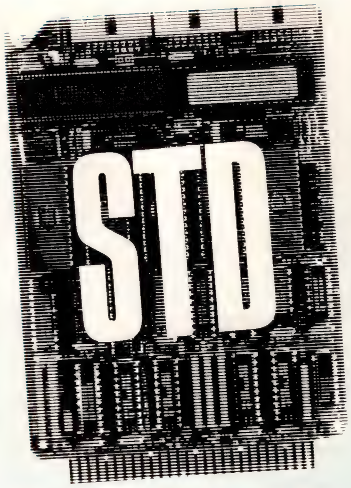

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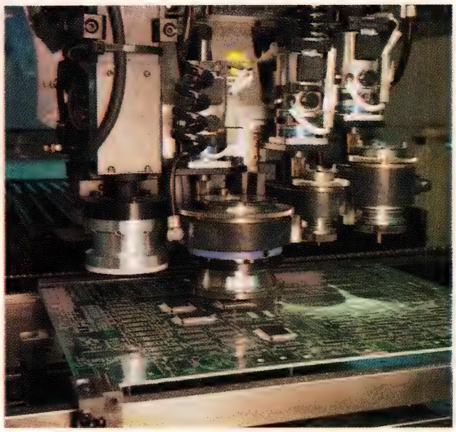

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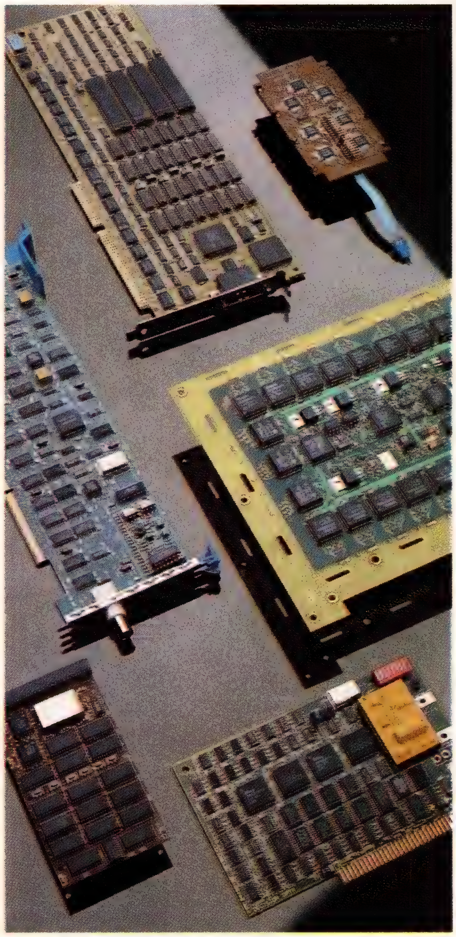

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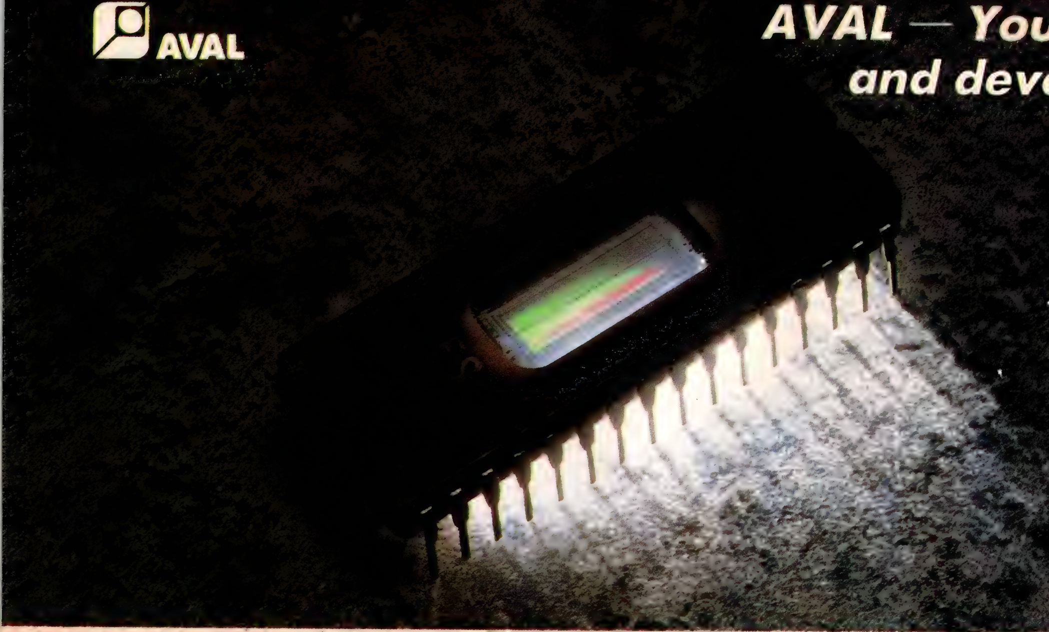


Multi-Megabit EPROM densities and expanding PLD architectures have spurred demands for innovations in programmer design. Aval Corporation, Japan's leading programmer manufacturer, now offers you a choice of development programmers for efficient and reliable programming at breakneck speeds. Our modular architectures adapt easily to support the broadest range of device families.

PKW-1100

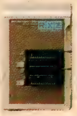
FLASH PROGRAMMER

Building on standards set by the universally successful PKW-1000 "Intelligent Programmer", AVAL's PKW-1100 "Flash" Programmer offers a quantum leap in performance to achieve tenfold reductions in Load-Verify times. Through interchangeable adapters, you can program EPROMs, EEPROMs, Microcontrollers, CMOS PROMs and EPLDs. The PKW-1100 uses manufacturer approved algorithms to maximize yields and reduce programming times. For ease of use, a large LCD and full menu driven command structure simplify the task of programmer setup and operation. For flexibility, Terminal and Online modes allow you to operate the PKW-1100 from a remote Terminal or Host.

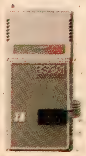
E(E) PROM
ADAPTER
RX 1

µ CONTROLLER
ADAPTER
RX 2

CMOS PROM
ADAPTER
RX 3



EPLD
ADAPTER
RX30



MULTI SET
ADAPTER
RX40

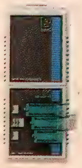
AVAL·PLUS

THE SYSTEM PROGRAMMER

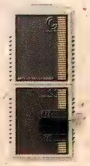
The AVAL-PLUS incorporates state of the art technology to support the broadest range of programming requirements. Programmable pin drivers, customised firmware and 16-Bit processing combine to eliminate overhead and ensure support for the fastest programming algorithms. With a choice of generic adapters, you can add device support as you need it. Options are available to program MOS Memories (EPROMs, EEPROMs, Microcontrollers and CMOS PROMs), Bipolar fusible PROMs and PLDs (PAL, EPAL, IFL, PLA, GAL etc.). As production and development tools, the powerful Multi-Set gang adapter and flexible ROM emulator options further enhance the profile of the AVAL-PLUS.

PLD
PROGRAMMER

MOS
PROGRAMMER

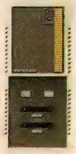


BIPOLAR
PROGRAMMER



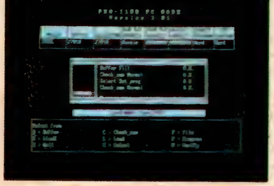
GANG SET
PROGRAMMER

MEGABIT ROM
EMULATOR



PCMODE SOFTWARE

PCMODE



PC-MODE software provides a user-friendly interface to your personal computer. A menu driven command structure and on-screen status simplify the task of programmer setup and file management. For design changes, the PC-MODE screen editor gives you direct access to your program code. It will also convert and output program files to your PC printer port in "AVAL Binary Format". In this format, Megabit data files can be transferred in under 25sec.

LOG/iC SYNTHESIS

LOG/iC

LOG/iC, the multipurpose design tool for universal logic synthesis, is available on most mini-and microcomputer systems. It lets you describe your design with an arbitrary mix of Equations, Truth Tables and State Machine Syntax. When you want to use graphic designs, LOG/iC's "Schematic Macro Library" supports input of netlists from third party schematic editors-such as OrCad. A Block orientated design syntax lets you define independent Macros and link them with these graphic blocks. LOG/iC's Functional Verifier then lets you simulate your design interactively on screen. The same input syntax can be optimised for different physical implementations.

AVAL CORPORATION

TOKYO HEADQUARTERS:
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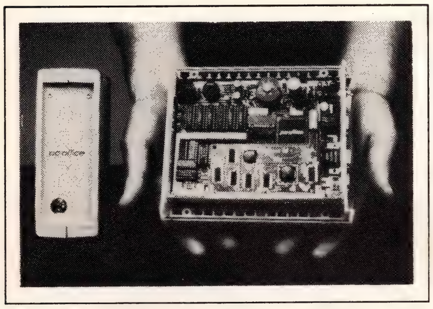
COMPUTERS & PERIPHERALS



LAN STATION

- *Includes complete IBM PC/XT-compatible computer*
- *Suits embedded applications such as point-of-sale terminals*

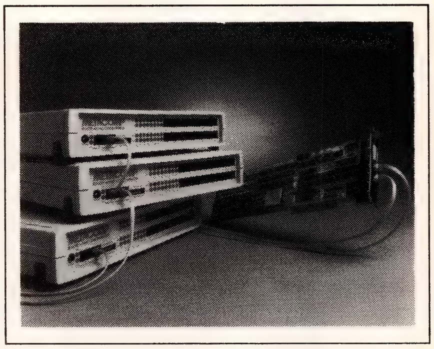
The ST/16 LAN-based IBM PC/XT-compatible station includes 768k bytes of RAM, keyboard interface, light-pen interface, and power supply, yet measures only 4.7×1.8×6.4 in. The product incorporates the Intel 2×4-in. Wildcard-88 CPU board that operates at 10 MHz. A half-length IBM PC/XT-compatible add-in slot allows OEMs to configure the LAN station for embedded applications such as factory automation and point-of-sale terminals. The diskless station includes an interface to the PC-Office LAN and can boot from a remote NetBIOS node. $195 to $495 (OEM qty).

PC-Office Inc, 4631 Viewridge Ave, San Diego, CA 92123. Phone (619) 268-3235. FAX 619-268-0126.

Circle No 368

I/O BOARD

- *Connects an IBM PS/2 to 128 asynchronous devices*
- *Uses a 16-MHz 80C186 µP and 512k bytes of DRAM*



The PSconnect adapter, an asynchronous communications subsystem for IBM's PS/2 models 50, 60, 70, and 80, connects the computer to as few as eight or as many as 128 asynchronous devices. The device fits into the host and uses a 16-MHz 80C186 µP and 512k bytes of dynamic RAM for storing and transferring data. The adapter also operates as a master or a slave on the Micro Channel Architecture bus. Supporting the Line Discipline 0 character for Unix, the unit reduces the host's terminal overhead. A single twisted-pair wire with RJ-45 connectors provides the connec-

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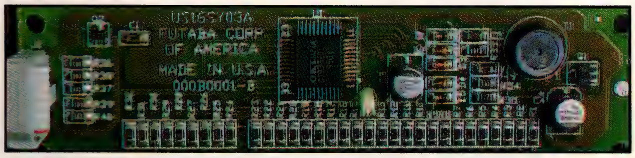

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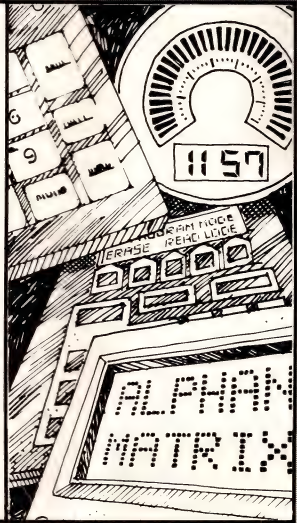

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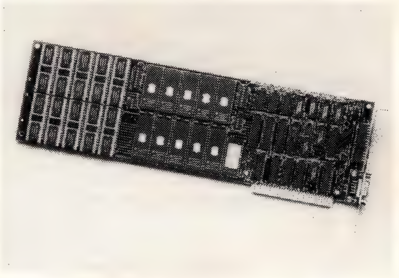
CIRCLE NO 139

tion between one or more host adapters and a remote asynchronous concentrator. The concentrator also contains a 16-MHz 80C186, comes with either eight or 16 RS-232C channels, and provides buffering and character processing for each port. The twisted-pair connection is compatible with the company's 2M-bps token-passing protocol. Adapter with software, $1835; 8- or 16-port RAC, $625 and $787, respectively.

Metacomp Inc, 15175 Innovation Dr, Suite A, San Diego, CA 92128. Phone (619) 673-0800. FAX 619-673-0321. TWX 910-335-1736.

Circle No 369



MEMORY BOARD

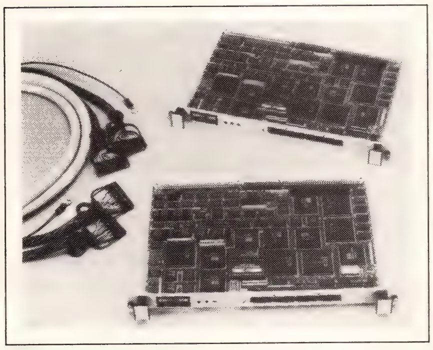
- *Provides virtual disk storage*
- *Emulates two floppy disks in 320k- to 1.2M-byte formats*

The V-disk virtual-disk memory board operates in an IBM PC, PC/XT, PC/AT, and compatible computers. The board can operate in harsh environments where conventional disk drives are undesirable. Available with either static RAM or EPROM, the device can emulate two floppy-disk drives in 320k-, 360k-, 720k-, or 1.2M-byte formats. A system with eight boards can also emulate a hard-disk drive with 20M bytes of storage capacity. A board installed with static RAM (SRAM) provides 10 times the access speed of a fast hard-disk drive, and a board with EPROM operates as a read-only disk. The board can also program EPROMs. 1.2M-byte EPROM, $665; 1.2M-byte SRAM, $1340; 2.4M-byte EPROM, $880;

2.4M-byte SRAM, $2230; no memory, $450.

Contec Microelectronics, 2010 N 1st St, Suite 530, San Jose, CA 95131. Phone (800) 888-8884; in CA, (408) 436-0340. FAX 408-436-0206.

Circle No 370



VME ADAPTER

- *Two VME systems communicate over shielded cable*
- *Built-in DMA controller transfers data as fast as 20M bytes/sec*

The Model 413 A32/D32 VME-VME adapter permits two VME systems to communicate with each other over a shielded cable. The cable is available in lengths as long as 25 ft. A 50-ft micro-coax cable is also available. The adapter features a built-in DMA controller that permits transfers from the memory of one system to the memory of the other system at speeds as high as 20M bytes/sec. In addition, a VME bus master in one chassis can execute random-access reads and writes to a destination chassis as though it were local memory. A page mode allows a bus master in the host system to access 32-bit data. An optional dual-port RAM lets the two VME systems communicate with each other through shared memory. The optional dual-port daughter board comes in 32k-, 128k-, and 1M-byte capacities. $3995.

Bit 3, 8120 Penn Ave S, Minneapolis, MN 55431. Phone (612) 881-6955. TLX 4997016. FAX 612-881-9674.

Circle No 371

SCAN CONVERTER

- *Converts display output display to NTSC or PAL format*
- *Automatically synchronizes on 21.5- to 35-kHz scan rates*

The RGB/Videolink 600 is a scan converter for the IBM PC and PS-2 computers as well as Apple's Macintosh II computer. The device auto-

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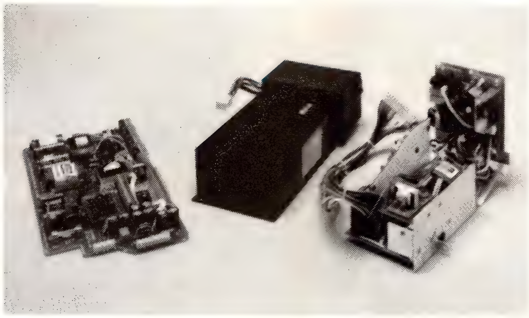

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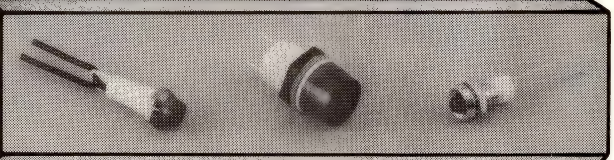

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CIRCLE NO 142

matically converts the graphics output of the computer display to NTSC or PAL (phase-alternation line) television format. The unit automatically synchronizes to IBM EGA (350 lines), IBM VGA (all modes), and Mac II (480 lines) systems. It synchronizes to scan rates in the 21.5- to 35-kHz range. A proprietary filter effectively eliminates flicker in the interlaced television output. The converter accepts full screen, noninterlaced RGB input signals and provides genlock, sync generation, and encoding for the output video. $10,000.

RGB Technology, 2550 9th St, Berkeley, CA 94710. Phone (415) 848-0180. FAX 415-848-0971.

Circle No 372

SCSI MULTIPLEXER

- *Enables a host to control as many as 24 peripherals*
- *Solid-state switch handles all SCSI data and command signals*

The SM-14 SCSI Bus Multiplexer expands the capacity of a SCSI bus system by enabling a host to control as many as 24 peripherals. A proprietary solid-state switch handles all the SCSI data and command signals from the host and switches them to one of four branches. As many as six peripherals with different identities can be connected to each branch. The multiplexer can communicate with a Common Command Set SCSI initiator in the host. When you use the company's DSC-202 SCSI analyzer/emulator as an initiator, application software uses the SCSI mode select commands to control the multiplexer switch. The software selects one of the four branches so that all attached peripherals become visible to the analyzer. $2840.

Ancot Corp, Mid-Peninsula Business Park, 1755 E Bayshore Rd, Suite 18A, Redwood City, CA 94063. Phone (415) 363-0667. FAX 415-363-0735.

Circle No 373

ACCELERATOR BOARD

- *Uses TMS320C30 DSP chip and plugs into IBM PC/AT*
- *Software permits C-compiled programs to run at 33M flops*

The Banshee/Spox floating-point accelerator board for the IBM PC/AT computer includes Spectron's Spox real-time operating system for its TMS320C30 DSP chip and a library of standard C language functions including optimized DSP and math subroutines. In addition, it contains a DOS shell, called Ashell, that links the system under control of the host, and a software package for developing real-time TMS320-C30 programs. Optional hardware includes the Banshee memory expansion board and I/O daughter boards. The unit's software package also permits C-compiled programs to run at 33M flops. Unit with 128k bytes of dual-access memory and complete software package, $6995.

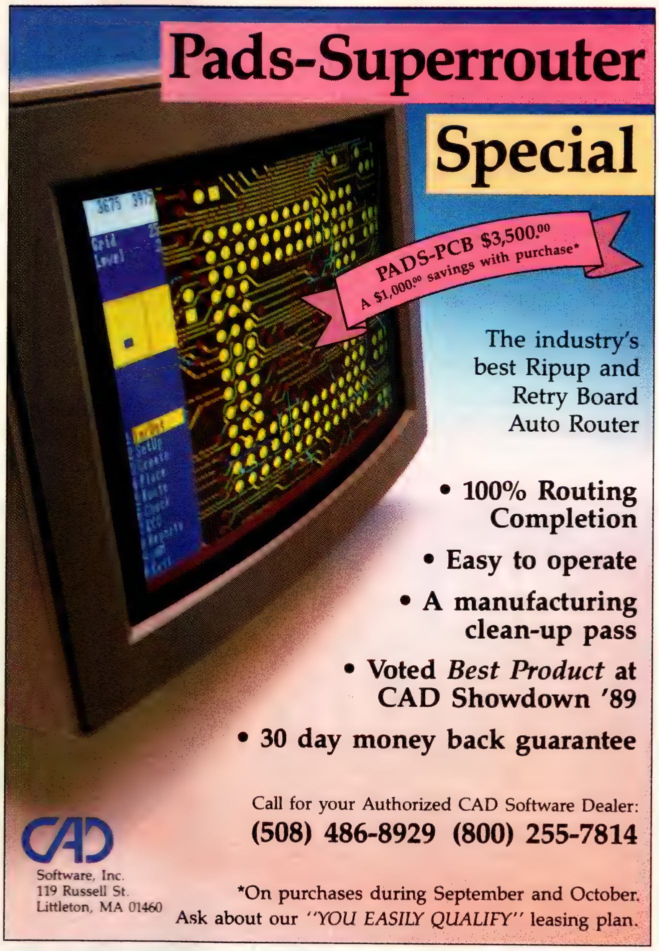
Atlanta Signal Processors Inc, 770 Spring St, Atlanta, GA 30308. Phone (404) 892-7265.

Circle No 374

PRINT CONTROLLER

- *Resides in IBM PC/AT or laser printer*
- *ASIC controls printing, interfacing, and memory management*

The ImageCard 8000 is a print controller card for laser printers. It is available in 2 configurations: the 8100 series, which resides in a Ricoh 1060 or Canon SX printer and the 8300 series, which resides in an IBM PC/AT compatible computer. The units come standard with HP's LaserJet II (PCL-4) emulation and



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CIRCLE NO 144

24 resident fonts. There are optional plug-in modules for fonts, emulations, memory expansion, or page description languages. The card uses a company-designed ASIC which controls virtually all the printing, interfacing, and memory management functions. The card also contains a 10-MHz 68000 µP, which enables print functions to occur in a background mode. The card costs from $250 to $275 with 512k bytes of DRAM and from $150 to $175 without memory.

Adaptec, 691 S Milpitas Blvd, Milpitas, CA 95035. Phone (408) 945-8600.

Circle No 375

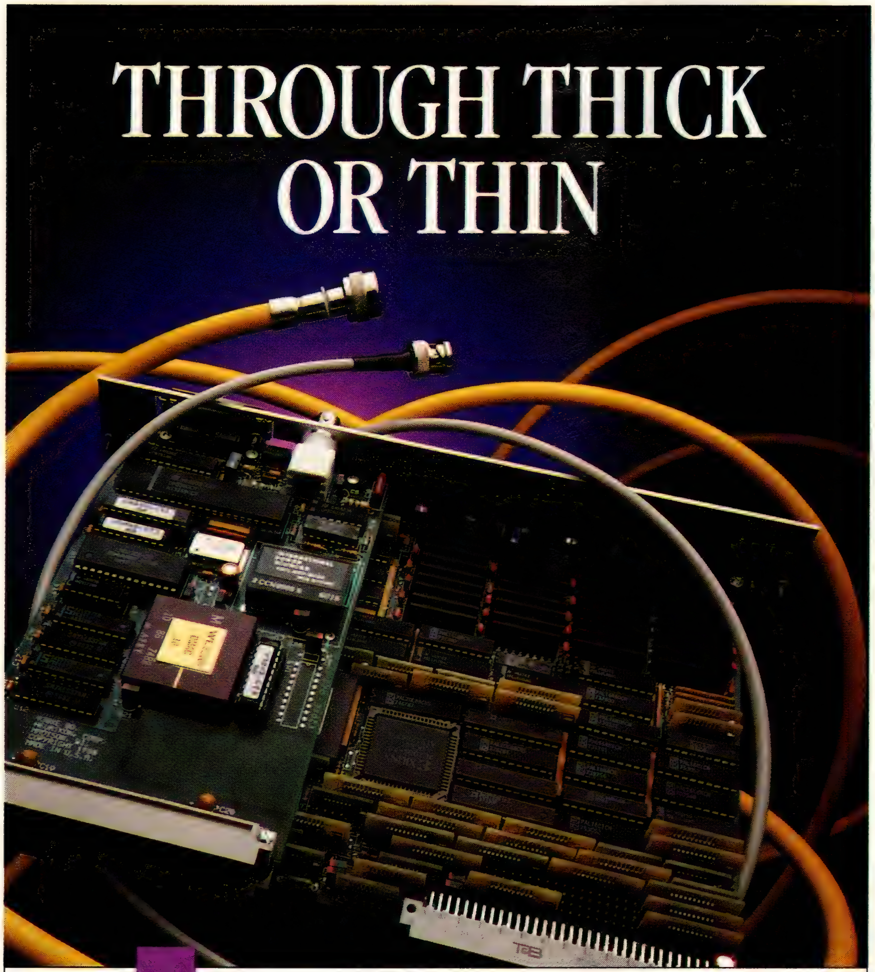
TRACKBALL

- *For IBM PC/XT/AT, PS/2, Apple II, and Macintosh*
- *Uses point-and-click action on an X and Y axis*

The RollerMouse trackball is designed to replace a conventional mouse used in IBM PC, PC/XT, PC/AT, PS/2, and Apple II and Macintosh computers. You point and click the device on an X and Y axis. The device features automatic acceleration that matches the speed of the ball to the cursor. The unit is 100% compatible with the Microsoft Mouse. Because the unit operates with 200-dpi resolution, it's compatible with desktop publishing and CAD/CAM/CAE software packages. The unit features a 4-button design where the two large buttons provide standard mouse-down operation, and the two small buttons lock the cursor in the down position for quick and easy drag across the screen. The device has a 5-in^2 footprint and a closed container that protects the ball from damage. $169.95.

Joystick Technologies Inc, 1225 Stone Dr, San Marco, CA 92069. Phone (619) 744-8546. FAX 619-744-1669.

Circle No 376



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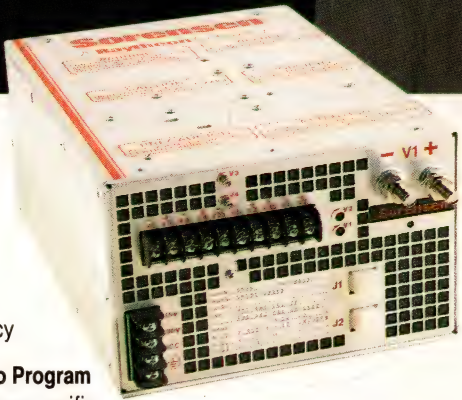

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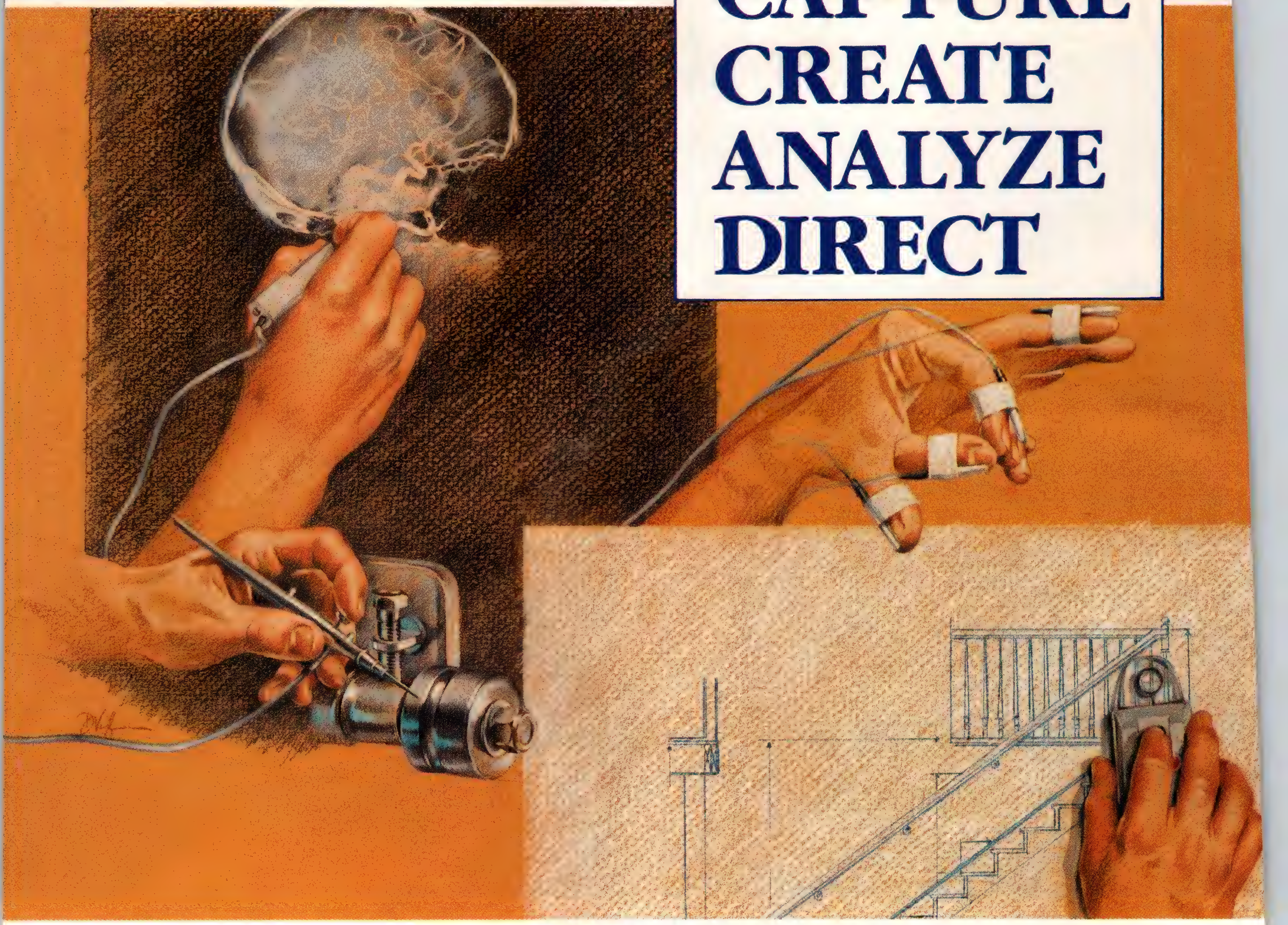

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OUTSTANDING ACHIEVEMENT AWARD

BUSCON show management, *Computer Design*, *EDN*, *ESD* and the Microcomputer Interface Group are proud to announce the BUSCON OUTSTANDING ACHIEVEMENT AWARD to be presented to the person deemed to have contributed most substantially to the growth and development of the board and systems level industry.

This award is yours to present. The following people have been nominated by a distinguished panel of editors consisting of John Miklosz of *Computer Design*, Jon Titus of *EDN* and David Wilson of *ESD*. We want your vote to determine the recipient of the BUSCON OUTSTANDING ACHIEVEMENT AWARD. Fill in and return the ballot coupon after making a selection or write in your own selection. The winner will be announced at the BUSCON BASH during BUSCON '90 West in Long Beach, CA this coming February.

Be part of this important industry wide event. Send in your vote today.

NOMINATIONS FOR THE 1989 BUSCON OUTSTANDING ACHIEVEMENT AWARD

Lym Hevle — Executive Director, VITA. Champion of open buses. One of the major Political movers behind Next Generation Architecture. Active in fostering open-bus approaches in both national and international markets. Instrumental in swaying military leadership to open buses.

Wayne Fischer — Marketing Director, Force Computers. Early backer and one of the authors of VMEbus specification. Chairman of VITA NGA Bridge committee, major proponent of Futurebus+. Active participant in major open-bus activities.

Ray Alderman — Vice President, Matrix Corp. President, ICOBA. Prominent industry spokesman, has directed International Board Level Symposium since inception, developed significant board-level market study.

Shlomo Pri-Tal — Motorola. One of the founding authors of VMEbus specification. Chairman of NGA technical committee, VME spokesperson, major proponent for the standardization of microcomputer architectures.

Paul Borril — Chairman IEEE Futurebus+ committee. Major proponent of open uses, worked in IEEE committees for almost all major bus architectures, major role in drafting of Multibus II specification, technical visionary in advance bus design.

Jim Ready — Board Chairman, Ready Systems. Early pioneer in packaged real-time kernels and development tools. Served on many open-bus committees, leading proponent of ADA for real-time systems.

John Hyde — Intel. Chairman, BUSCON technical committee, leading spokesman for Multibus II, active participant IEEE Futurebus+ committee, advocate of unified approach for open-bus architectures, leader in bridging MMG and VITA in next-generation approaches.

My vote for the 1989 BUSCON OUTSTANDING ACHIEVEMENT AWARD is: (must be received by January 15, 1990.)

____

My write-in nomination is: _______________________________
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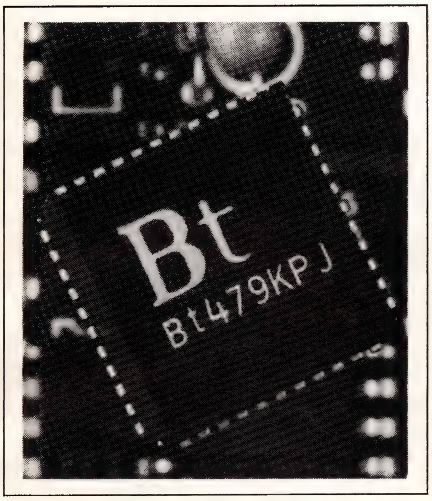
INTEGRATED CIRCUITS



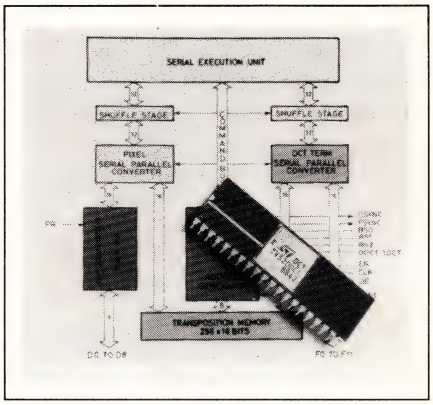
RAMDAC

- *Has three 8-bit D/A converters*
- *Contains four 256-color palettes*

The Bt479 RAMDAC overcomes the inability of today's PCs to support multiple applications and multiple windows simultaneously with unique color selections. The Bt179 enables high-end PCs to display as many as 16 windows, each capable of accessing one of four available 256×24-color palettes. The Bt479 supports as many as 1024 simultaneous colors through the 1k×24-color palette RAM and triple 8-bit D/A converters. To solve the problem of overlapping windows, the Bt479 features a window-priority encoder that automatically prioritizes the windows on a pixel-by-pixel basis via stored location and priority settings. The Bt479 supports IBM VGA, enhanced VGA, and 8514A graphics standards. Bt479 35-MHz version in a 44-pin plastic leaded-chip carrier, $29 (100).

Brooktree Corp, 9950 Barnes Canyon Rd, San Diego, CA 92121. Phone (619) 452-7580. FAX 619-452-1249. TLX 383496.

Circle No 397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D0 TO D8
F0 TO F11

DEDICATED DSP CHIP

- *Performs discrete cosine transforms*
- *Suitable for image-compression*

The STV3200 is a dedicated DSP µP that contains all the circuitry required to perform a forward or inverse discrete cosine transform (DCT) at pixel rates to 13.5 MHz. A DCT transforms a block of pixels, typically ranging from 4×4 to

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CIRCLE NO 150

16×16, into a block of coefficients in such a way that almost all the picture information is concentrated in a small number of coefficients. In this way, very high compression ratios are possible without an appreciable loss of image quality when the picture is reconstructed. The STV3200 consists of two main functional blocks: a pipelined execution unit and a transposition memory. Using a fast algorithm and serial arithmetic, the execution unit performs a direct or inverse DCT on a 16×16-bit data vector. Depending on the chosen block size, this corresponds to one 16-point, two 8-point, or four 4-point transforms. The transposition memory, which contains a 4096-bit static RAM, holds the intermediate results of the 2-pass algorithm. The STV3200 has two bidirectional I/O ports: a 9-bit pixel port and a 12-bit coefficient port. Control pins select forward or inverse operation and the pixel data format. Housed in a 40-pin DIP, the STV3200 operates from a single 5V supply. $360 (1-9).

SGS-Thomson Microelectronics, 1000 E Bell Rd, Phoenix, AZ 85022. Phone (602) 867-6100. FAX 602-867-6290.

Circle No 398

A/D CONVERTER

- *Includes T/H circuit*
- *Operates at 2 MHz*

The ADC-00305 is a 12-bit, 2-MHz (500 nsec) A/D converter. Included in the hybrid is a track and hold circuit, data registers, 3-state output buffers, and timing circuits. The ADC-00305, which interfaces to most CPUs, provides nine bipolar/unipolar, jumper-selectable analog-input ranges. Because all timing is self contained, the converter needs only an encode command to start its conversion cycle. The ADC is packaged in a 40-pin DIP and operates over the 0 to 70°C temperature range. From $385. Delivery, stock to six weeks ARO.

ILC Data Device Corp, 105 Wilbur Pl, Bohemia, NY 11716. Phone (516) 563-5678. FAX 516-567-7358. TWX 510-228-7324.

Circle No 399

MICROPROCESSOR

- *Contains 2k bytes of SRAM*
- *Includes clock-generator/controller*

The Z84C50 μP combines the Z80 8-bit μP, 2k bytes of static RAM, and a clock-generator/controller on a single chip. Operating at 10 MHz, the Z84C50 also features an on-chip wait-state generator for the automatic insertion of wait states to

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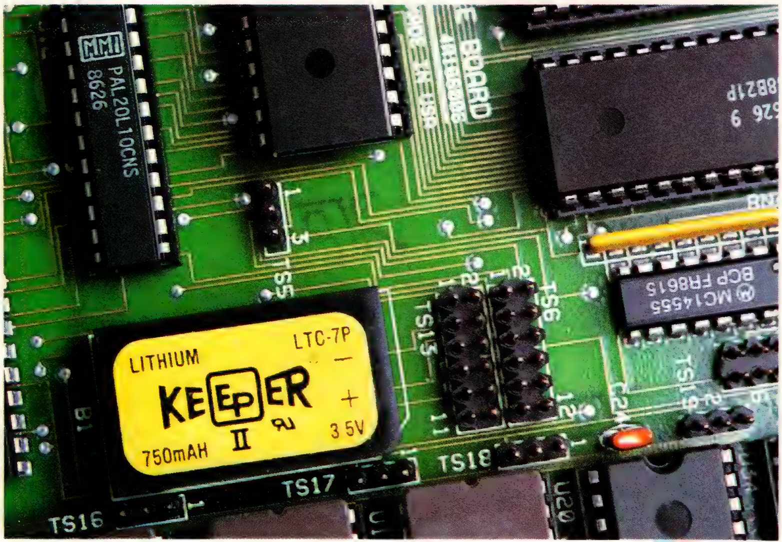

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CIRCLE NO 145

synchronize the µP with external memory or peripherals. Using the Z80's set of 158 instructions, the Z84C50 features direct pin and code compatibility with the Z80. The Z84C50 retains other popular features such as a built-in accumulator, a dual-register set that allows high-speed context switching, and index registers for additional memory-addressing flexibility. In addition, the device includes a built-in ALU, bus control, and timing-control circuits. The Z84C50 is available in a 40-pin DIP, a 44-pin plastic leaded-chip carrier, and a 44-pin quad flatpack. $6 to $7 (1000).

Zilog Inc, 210 Hacienda Ave, Campbell, CA 95008. Phone (408) 370-8000. FAX 408-370-8027.

Circle No 400

MILITARY DSP CHIP

- *Processed to MIL-STD-883*
- *Has 12.5-MHz speed*

Processed to MIL-STD-883, the ADSP-2100 DSP µP is now available to military contractors and defense agencies in a 12.5-MHz version. According to the company, the 80-nsec instruction cycle and dual-port Harvard architecture make the ADSP-2100AU the fastest programmable DSP µP available for military applications. The device can compute a 1k-point FFT in 2.94 msec. In addition to the 12.5-MHz device, three slower versions of the ADSP-2100 are now available as standard military drawings (SMDs). An SMD listing simplifies device selection and purchasing: Defense agencies can now use the 6-, 8-, and 10-MHz versions of the ADSP-2100 and ADSP-2100A without having to create a custom drawing. To reduce space requirements the ADSP-2100 is packaged in a 100-lead, surface-mount ceramic quad flatpack. From $462 (100).

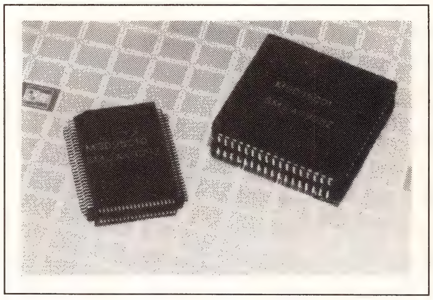
Analog Devices, Box 9106, Norwood, MA 02062. Phone (617) 461-3672.

Circle No 401

ESDI INTERFACE

- *Supports the IBM MCA bus*
- *Provides handshaking for ESDI drives*

The MSD95C10 MIDAS (Micro Channel Interface for Disk Access) chip provides all the handshaking signals required by the IBM MCA (Micro Channel Architecture) bus



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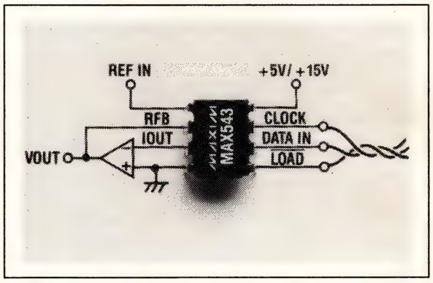
and the serial interface logic for ESDI disk drives. Although optimized to interface with the previously announced MSD95C01 disk controller, the MIDAS chip ensures bit- and register-level compatibility with the IBM PS/2 ESDI adapter, regardless of the hard-disk controller and local processor used. The MIDAS chip can interface to an 8-bit disk controller and transparently perform the appropriate byte swapping, allowing the controller to access a 16-bit-wide buffer. The local processor interface includes a dedicated 8-bit multiplexed bus and the associated control lines, which provide the processor with both the reset and interrupt functions. The MSD95C10 MIDAS chip comes in a 100-pin quad flatpack. $20 (5000).

Standard Microsystems Corp, 35 Marcus Blvd, Hauppauge, NY 11788. Phone (516) 273-3100.

Circle No 402



MULTIPLYING DAC

- *Features 12-bit resolution*
- *Has 3-wire serial interface*

The MAX543 12-bit DAC, which features a 3-wire serial interface, is available in either an 8-pin miniature DIP or a 16-pin SO package. These small-sized packages reduce board space and system complexity by decreasing the footprint area and the number of signal traces on a circuit board. The MAX543, which works with a 5 or 15V supply, has ±1 LSB gain error and ±½ LSB relative accuracy, and has guaranteed monotonicity over its operating temperature range. Even though the DAC comes in a small package, it features a separate clock input and load-DAC control pins. All digital inputs in the device are TTL and CMOS compatible. The MAX543 is available in three temperature ranges. From $8.50 (100).

Maxim Integrated Products, 120 San Gabriel Dr, Sunnyvale, CA 94086. Phone (408) 737-7600.

Circle No 403

TRACK-AND-HOLD IC

- *Features 12-bit accuracy*
- *Large-signal bandwidth is 70 MHz*

With a settling time to 0.01% of 25 nsec, the CLC942 track-and-hold IC

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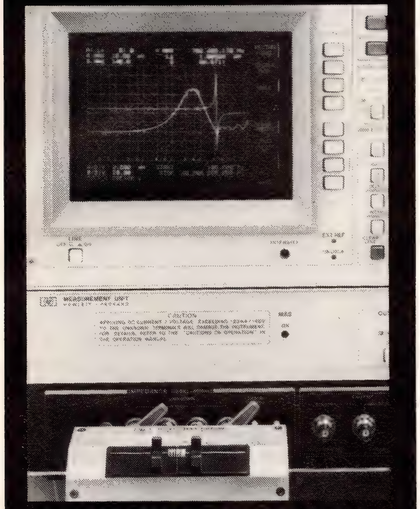

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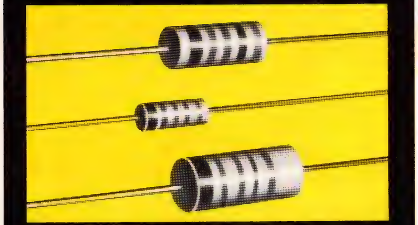

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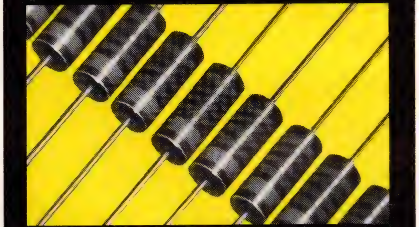

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provides 12-bit performance with a sampling capability to 20M samples/sec. The CLC942's input and output buffer amplifiers combine with a low-jitter sampling bridge to provide stable operation. Other important parameters include 1.4-psec (rms) aperture jitter, second-harmonic distortion of –74 dBc at 4 MHz and –50 dBc at 20 MHz, and third-harmonic distortion of –75 dBc at 4 MHz and –64 dBc at 20 MHz. The feedthrough rejection ratio is –78 dB at 20 MHz. The CLC942 comes in a 24-pin, side-brazed ceramic package. From $139 (100).

Comlinear Corp, 4800 Wheaton Dr, Fort Collins, CO 80525. Phone (303) 226-0500. FAX 303-226-0564. TLX 450881.

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- *For thin-film recording heads*
- *Features low-noise read preamp*

The SSI-32R524R is a bipolar read/write IC designed for use with 2-terminal, low-inductance thin-film recording heads. The IC features a maximum input noise of 0.75-nV/$\sqrt{\text{Hz}}$ with a maximum input capacitance of 60 pF. The 32R524R provides a low-noise read preamp and write control for as many as eight channels. A power-supply fault-protection circuit disables the write-

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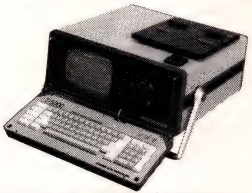

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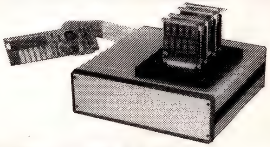

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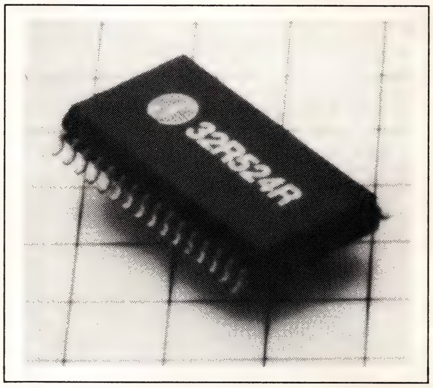

current generator during power sequencing. In addition, the IC improves write-to-read recovery times by controlling the common-mode output shift when switching from write to read mode. The IC requires 5 and 12V supplies and is available in a variety of surface-mount packages. $16 (1000).

Silicon Systems, 14351 Myford Rd, Tustin, CA 92680. Phone (714) 731-7110.

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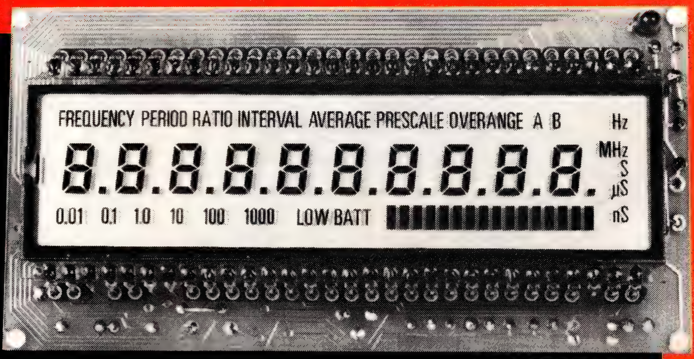
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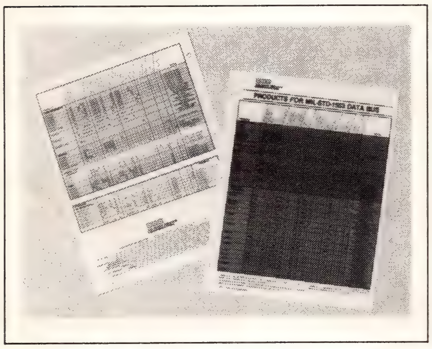
CIRCLE NO 157

Explore and apply source-measure units

A booklet describes the basic technology of source-measure units and an applications handbook details 24 typical source-measure test configurations. The 24-pg tutorial handbook describes a source-measure unit, how it works, how to design test systems, and how to sample test setups. The handbook also features a glossary and outlines the advantages of source-measure units. The applications overview book deals with 24 common source-measure applications, including MOSFET, GaAs, and bipolar measurements, diode and oxide characterization, and various research and electronic manufacturing test examples.

Keithley Instruments Inc, 28775 Aurora Rd, Cleveland, OH 44139.

Circle No 388

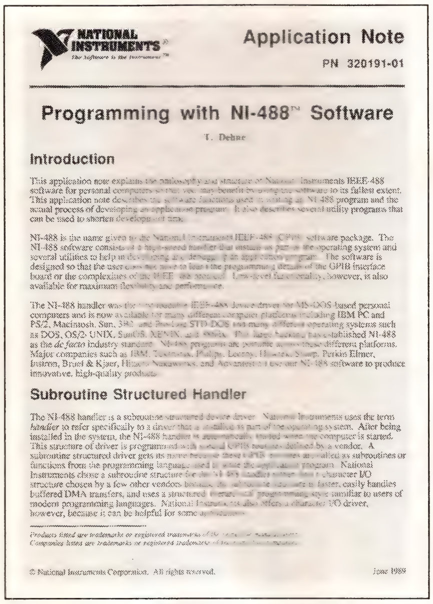


Handy chart lists MIL-STD-1553 products

This product-selection chart highlights more than 50 data-bus products. The color-coded, 2-sided chart provides a guide to more than 30 MIL-STD characteristics. Product categories include transceivers, complete terminals, card assemblies, testers, and special test equipment. The table comes with three punched holes so you can insert it in a loose-leaf notebook for easy reference.

ILC Data Device Corp, 105 Wilbur Pl, Bohemia, NY 11716.

Circle No 389



Application Note

PN 320191-01

Programming with NI-488™ Software

T. Dehne

Introduction

Subroutine Structured Handler

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June 1989

Programming with IEEE-488 software explained

Programming with NI-488 Software explains the philosophy, structure, and features of the company's NI-488 software. The 8-pg note helps users improve the performance of controlling instrumentation and minimize application development time. Several time-saving utilities described include an interactive control program, a configuration utility, the universal language interface for HP-style calls, and diagnostic programs.

National Instruments, 12109 Technology Blvd, Austin, TX 78727.

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Guide to structured systems analysis

This guide provides the latest beliefs about and applications of structured systems analysis and design. The first part summarizes 66 English-language papers published since 1984 and is grouped into a general review; applications and case studies; real-time systems; structured systems analysis and design; and prototyping. The second part includes details of books, market reports, UK academic research, software-tool suppliers, UK consultants, and training courses provided by both publicly funded and commercial organizations. £31.

IEE, Box 26, Hitchin, Herts, SG5 1SA, UK.

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Catalog lists packaging and hardware

This issue of the company's catalog features its latest versions of MultibusI/II and VMEbus wire-wrapping boards and services, as well as prototype and extender cards and covers. The publication covers several Multibus boards, including universal pattern wire-wrapping with 2- or 3-level wrap posts, and socket boards that are suitable for wire wrapping or soldering. The publication also describes the company's complete wiring services.

Scanbe, 6790 Flanders Dr, San Diego, CA 92121.

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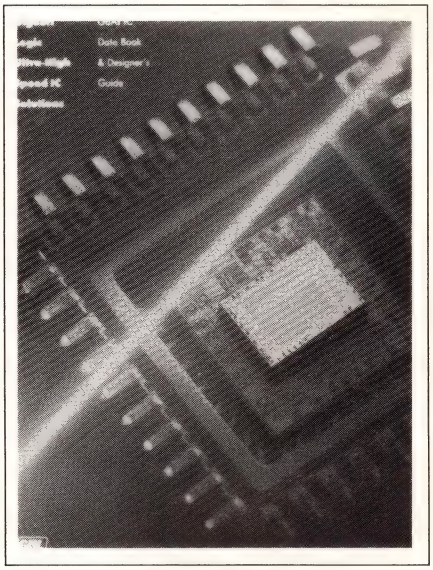

Book on GaAs ICs

The 480-pg *GaAs IC Data Book* offers information about the company's standard PicoLogic, NanoRam, NanoRom, and fiber-optic communications families. It also covers standard cell arrays for developing low-power, high-performance VLSI ASICs having 15,000 gates, and provides information about foundry services, prototyping products, packaging, testing, and reliability.

Gigabit Logic, 1908 Oak Terrace Lane, Newbury Park, CA 91230.

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Equipment for testing RF and EMI

Total RFI/EMI/EMC Interference Control Services covers the company's Certified Testing program that determines compliance with commercial and military electromagnetic-compatibility specifications. The brochure describes RF and ESD tests in the frequency range of 20 Hz to 18 GHz. Also included are computer-controlled evaluations of shielded enclosures, cabinets, and other facilities for magnetic and electric fields and plane-wave attenuation. The publication provides information about the company's EMC consulting, design, and software development capabilities.

Instrument Specialities Co Inc, Delaware Water Gap, PA 18327.

Circle No 393

Journal on real-world signal processing

Analog Dialogue presents information about circuits, systems, and software for real-world signal processing. This issue covers the ADSP-2101, a monolithic CMOS microcomputer optimized for digital signal processing. Other applications-oriented articles in this issue focus on an isolated strain-gauge module, two 6-bit monolithic flash ADCs, and a fast-slewing monolithic op amp with a wide bandwidth. The "Ask the Applications Engineer" column, which addresses user questions and problems, discusses V/F converters.

Analog Devices, Literature Center, 70 Shawmut Rd, Canton, MA 02021.

Circle No 394

Standard for ADC and DAC terms, definitions, symbols

This expanded 38-pg reference is suitable for educators, technical writers, and users and manufacturers of A/D and D/A converters. *Terms, Definitions, and Letter Symbols for Analog-to-Digital and Digital-to-Analog Converters* (JESD-99-1-1989,) (which sells for $15,) provides numerous illustrations and defines general terms, static-performance terms, dynamic-performance terms, and error terms in alphabetical order. The addendum re-

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vises and replaces a part of the existing JEDEC Standard No. 99, *Glossary of Microelectronic Terms, Definitions, and Symbols* (JESD99-1985,) which is available for $23.

EIA Standards, 1722 Eye St NW, Suite 300, Washington, DC 20006.

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What you need for computer/electronic repair

A 66-pg catalog presents tools and equipment for computer and electronic repair. Among the product listings are breakout boxes; interface testers; connector kits and tools; static-control wrist straps; oscilloscopes and replacement scope probes; and DVMs and accessories. The extensive coverage includes product descriptions with illustrations and detailed price information.

Specialized Products Co, 2117 W Walnut Hill Lane, Irving, TX 75038.

Circle No 395

Designing multiple-order bandpass filters

Application note AN27A presents a simple method of designing multiple-order all-pole bandpass filters. The publication provides a brief tutorial on bandpass-filter theory, hardware implementation of designs, and tables to use in designing Butterworth and Chebyshev bandpass filters. The note also discusses the factors involved in the choice of a Butterworth vs a Chebyshev filter approach.

Linear Technology Corp, 1630 McCarthy Blvd, Milpitas, CA 95035.

Circle No 396

Evaluation of 3-D CAD software

The 250-pg report, *PC CAD Comparison*, provides a comprehensive technical evaluation of the top seven mechanical-engineering software packages. Reviewing AutoCAD, Micro Cadam, CADkey, Personal Designer, Microstation, Anvil-5000, and VersaCAD, the publication measures how well these seven leading systems perform 800 different functions in eight categories. The study also evaluates the software based on its performance in five benchmarks simulating real-world mechanical-engineering environments. $465.

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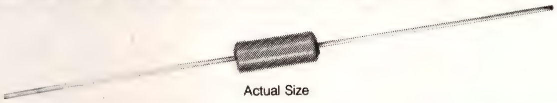

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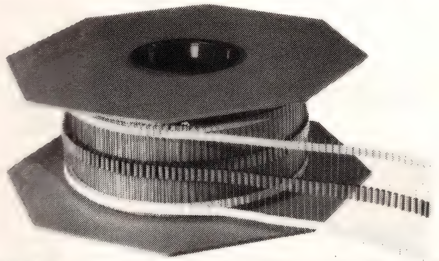

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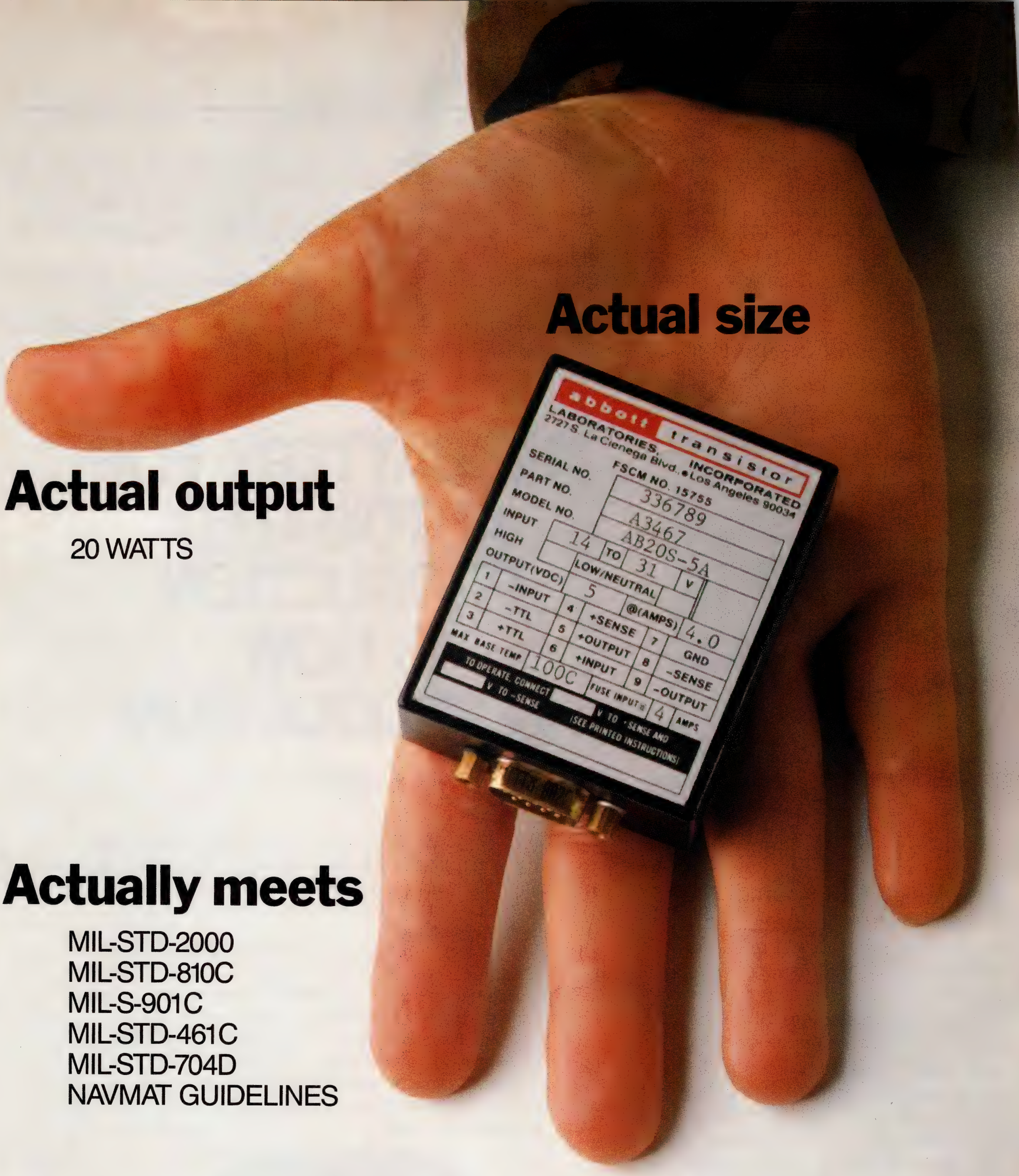

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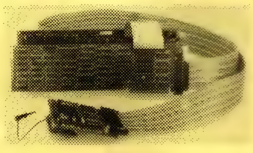

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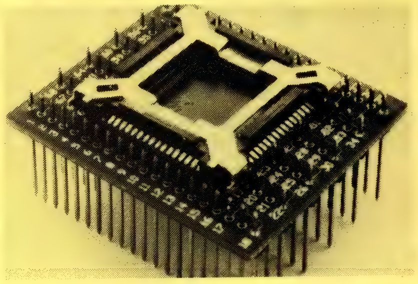

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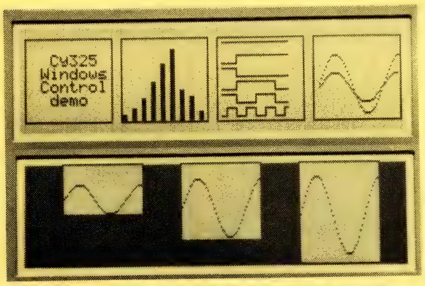

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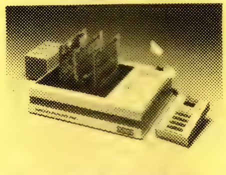

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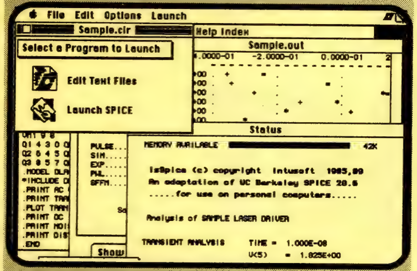

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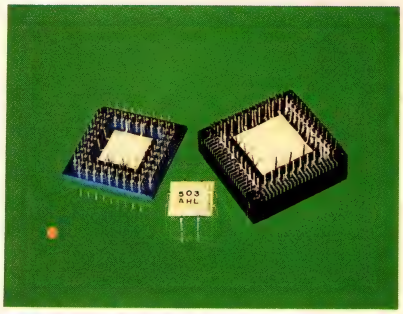

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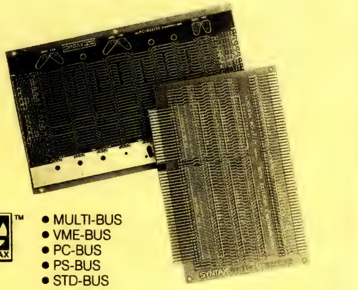

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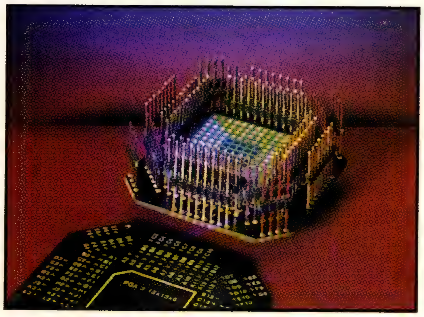

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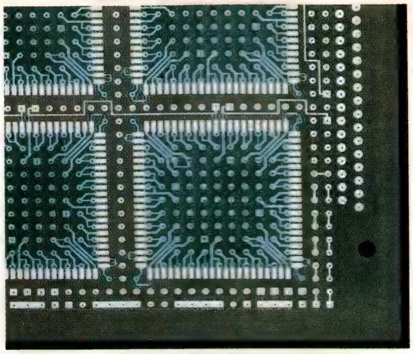

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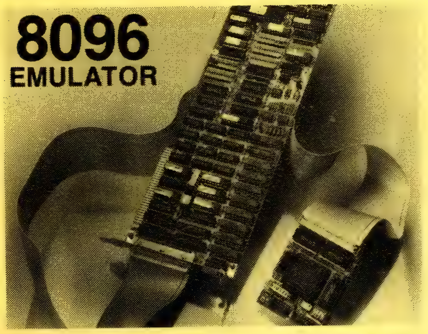

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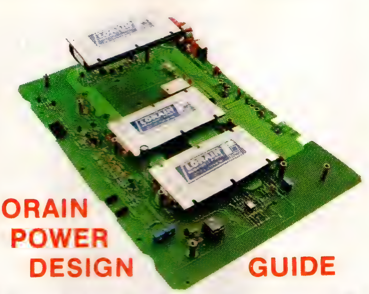

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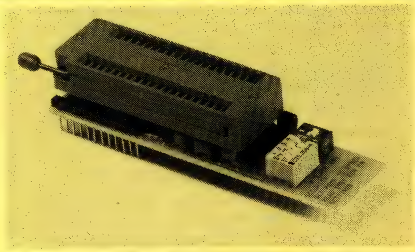

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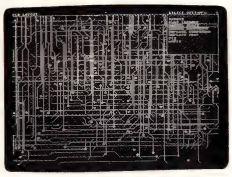

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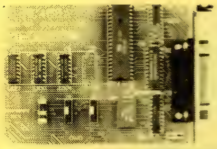

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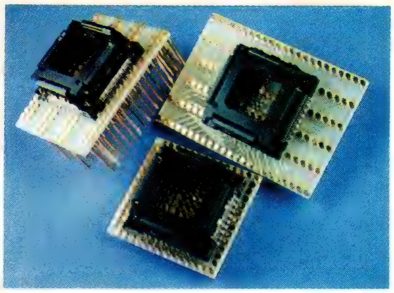

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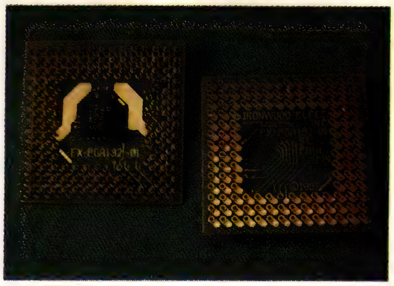

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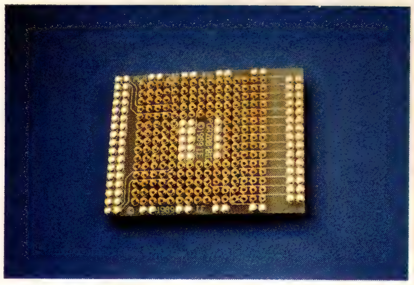

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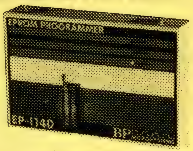

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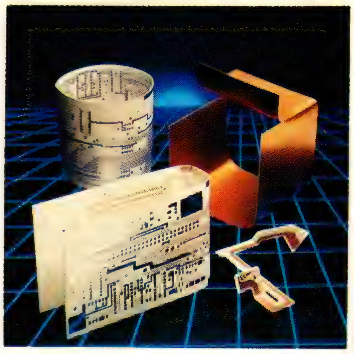

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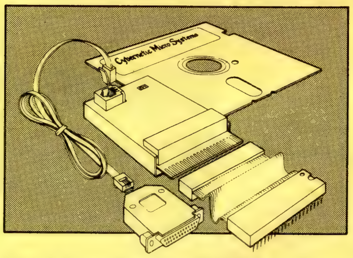

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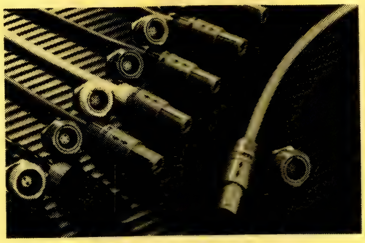

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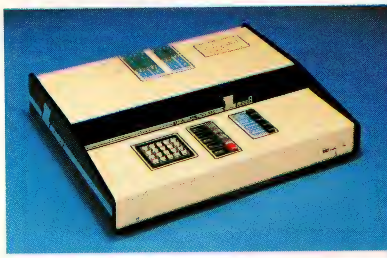

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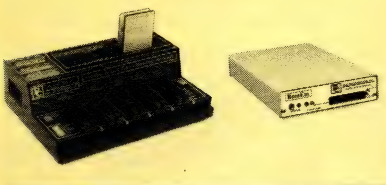

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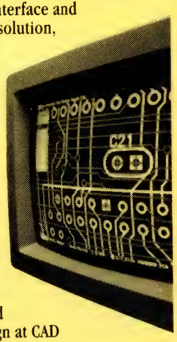

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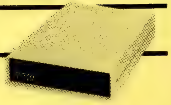

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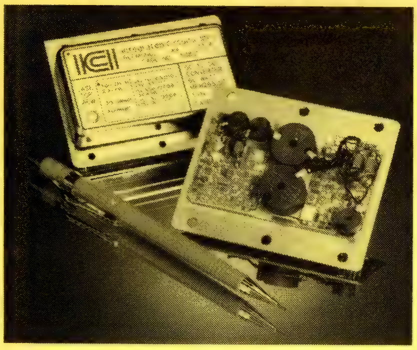

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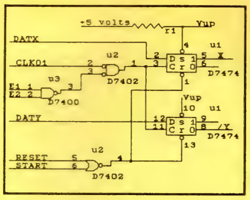

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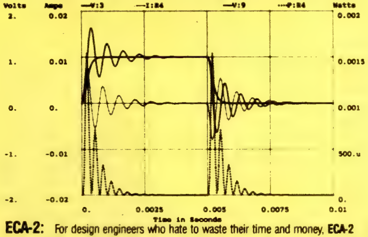

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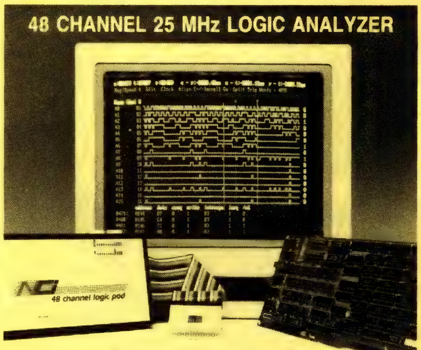

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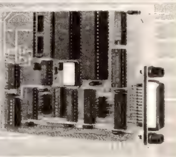

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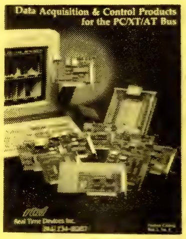

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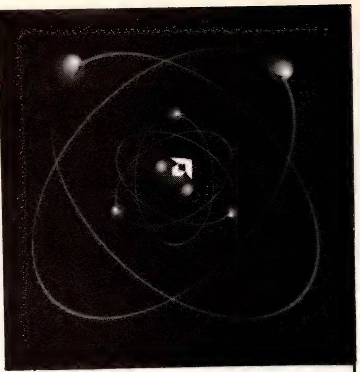

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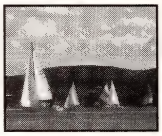
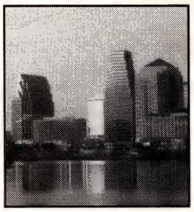

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BRIEFINGS

Modules yield denser systems

SipStik modules plug perpendicularly into Micro-Edge connectors residing on custom motherboards.

Preassembled subsystems, connectors, and motherboards save space

WILL DAVIES
Dallas Semiconductor Corp

A different approach to modularity lets you build custom, µP-based systems out of pretested elements that snap together like an erector set and yield a functional density that can't be achieved using surface-mount technology.

Three components make up these high-density electronic systems: silicon-intensive substrates that form modular electronic subsystems the size of a stick of chewing gum; surface-mount planar motherboards; and recent connector advances.

The preassembled, pretested subsystems—called SipStiks—are leadless substrates of electronic components that offer the rough functional equivalent of daughterboards in conventional pc-board/bus/backplane computer systems. The SipStiks mate with AMP Micro-Edge single in-line connectors residing on motherboards to form 3-tier systems based on Eurocard standards.

Three basic steps

By taking this modular approach to designing a system architecture, the engineer can reduce design time. After making a catalog selection of SipStiks, the designer need only lay out the motherboard and plug the SipStiks (tier 1) into the connectors on the motherboard (tier 2). With or without an enclosure, the motherboard can be fitted to a rack and backplane (tier 3).

The motherboard size is defined as a standard single Eurocard measuring 100 × 160 mm. This size lets you mount 12 SipStik products, which yields as much as a fivefold increase over traditional, single-sided surface-mount packing densities. It provides sufficient area for more than 50 million transistors using currently available components.

Because the system uses the Eurocard form factor, standard racks and backplanes provide for system expansion beyond the motherboard. The result can be very complex systems built from standard SipStiks that are made specific to an

IC makers grapple with metastability

Within the last few months, at least two IC makers have introduced metastable-resistant logic devices, and more such products are on the way, say manufacturers. The metastable-resistant parts help reduce the chances that flip-flops will go into a metastable state. In addition, the parts' data sheets give designers the information needed to design around such metastable states when they do occur.

Metastability occurs when designers try to synchronize digital signals of different frequencies to a local clock, according to an explanation by Texas Instruments (Dallas, TX), one of the companies introducing metastable-resistant parts. In such applications, designers cannot guarantee that clock and data signals will not violate the setup and hold times published in flip-flop data sheets. When setup and hold times are violated, a flip-flop's output can become metastable—either oscillating or stuck between 0 and 1. The condition can cause logic errors or false clocking throughout a system.

Metastability has always

A call for Ada experts

Although Ada's popularity is growing slowly, the demand for experts exceeds the supply

MICHAEL BALL
Contributing Editor

Over the last two and a half years, the number of Ada projects in the US has increased eightfold, according to the Department of Defense's Ada Joint program office. And if predictions are on

EDN Magazine Edition
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A Partnership in Power and Prestige Worldwide

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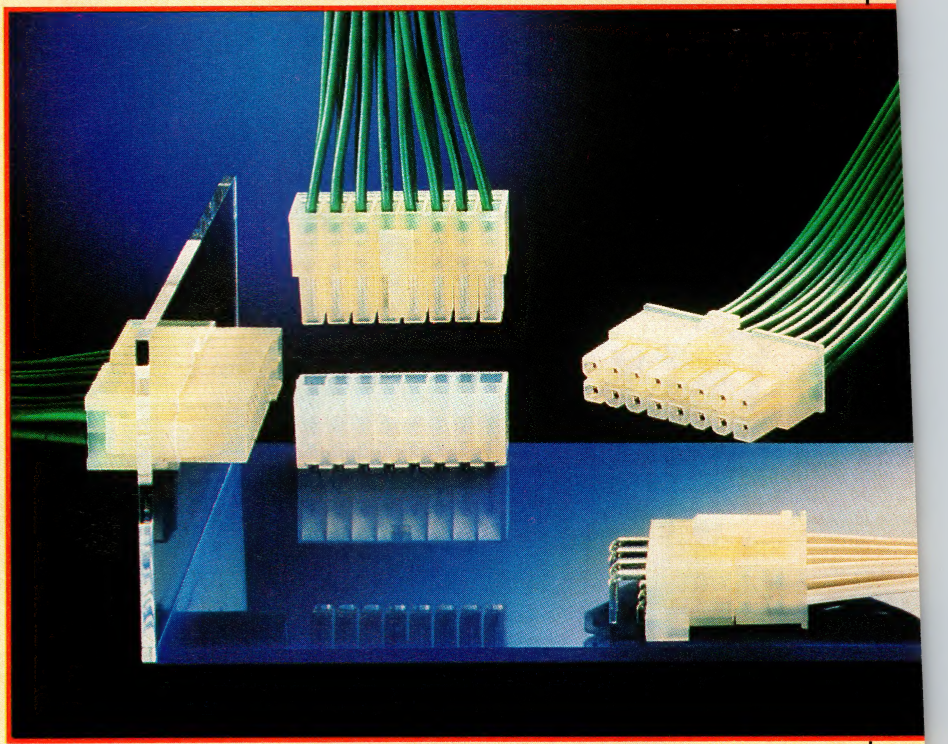
HIGH CURRENT & HIGH DENSITY



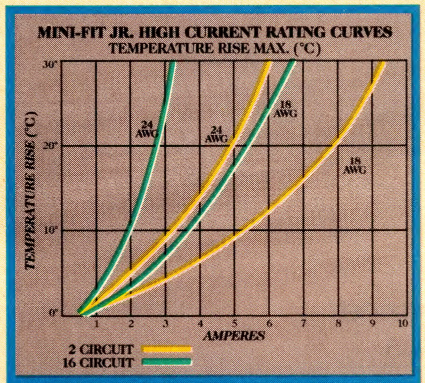
Mini-Fit Jr. is our new generation power connector for your panel-to-wire, wire-to-wire, and board-to-wire applications.

From power supply to power distribution, Molex makes the connection.

Molex, the industry leader, now offers the most complete line of pin and socket connectors available. From standard wire-to-wire and wire-to-board versions, to the new high-performance "Mini-Fit Jr."

Mini-Fit Jr. meets today's demand for miniaturized design components.

With current handling capability of up to 9 amps per circuit, and a connector mating force of only 1.54 pounds per circuit, the Mini-Fit Jr. offers the ideal solution to your high current and high density interconnection requirements.



Mini-Fit Jr. can handle high current (up to 9 amps) despite its small size.

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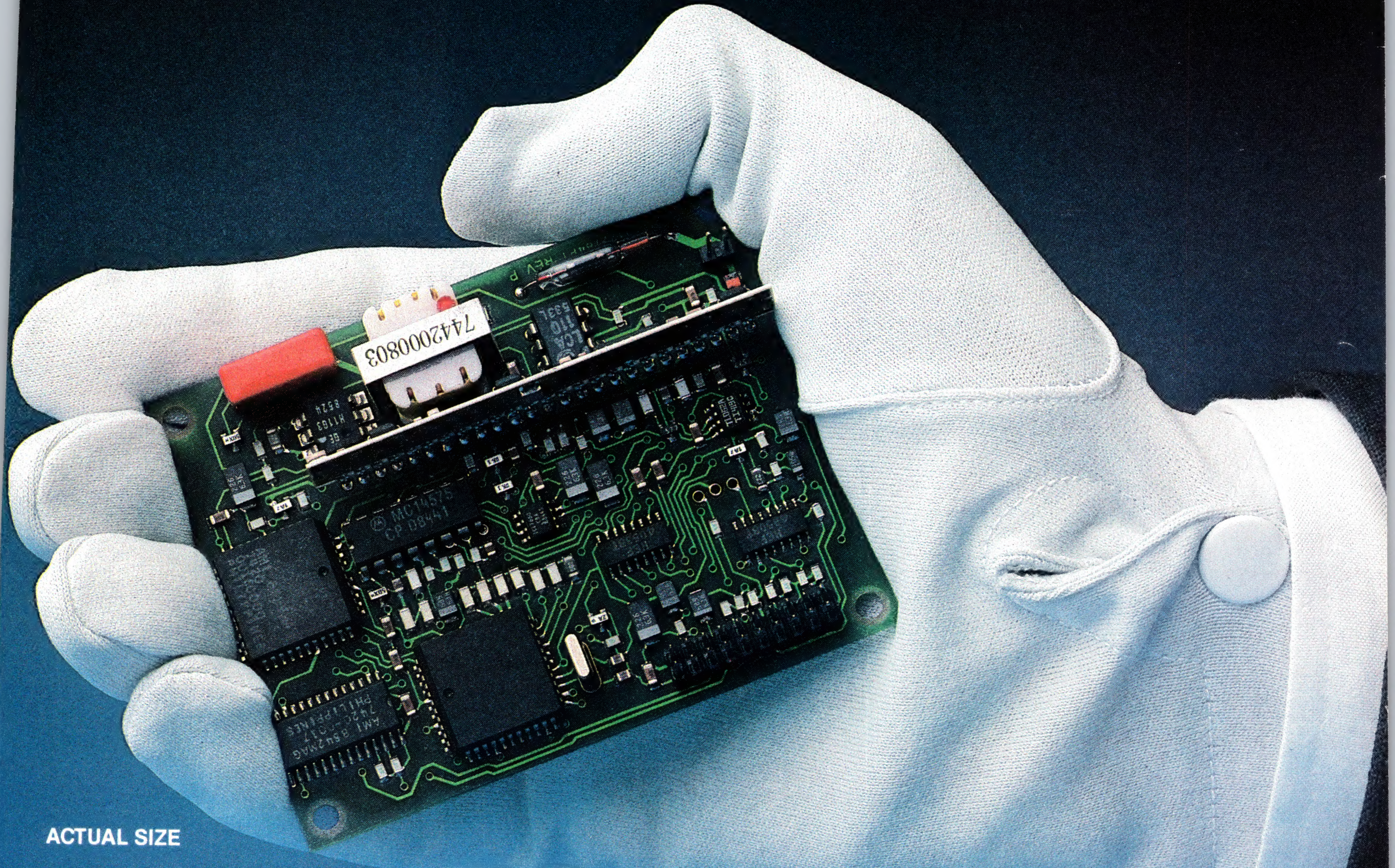
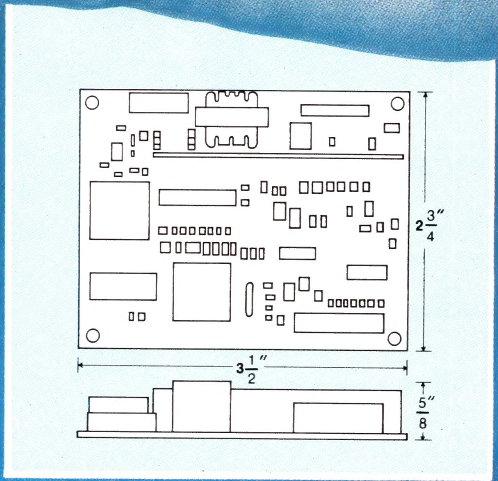
MODEM DESIGN ELEGANCE AT 2400 BPS





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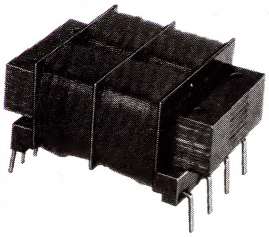

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- 5 through 230V outputs; at 10mA through 9.6A; 2.5 VA through 48 VA
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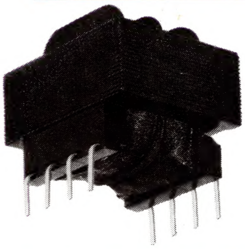

- Smaller footprint for maximum PC board component density
- 50/60 Hz…115V or 115/230V primary
- 5 through 120V outputs; at 10mA through 7.2A; 1.1 VA through 36 VA

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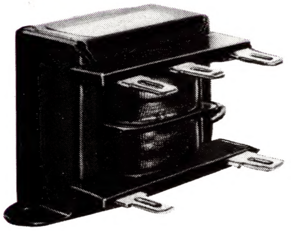
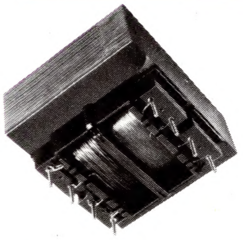


- Chassis mounting
- Solder *and* quick-connect terminals
- 50/60 Hz…115V or 115/230V primary
- 10 through 120V center-tap outputs; at 20mA through 10A; 2.4 VA through 100 VA

THE ONE-4-ALL™ SERIES



- VDE certified
- UL recognized and CSA certified
- Dual primary…115/230V, 50/60 Hz
- 5 through 36V outputs; at 70mA through 11.2A; 2.5 VA through 56 VA

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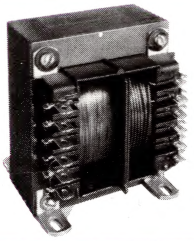

- VDE certified
- UL recognized and CSA certified
- Chassis mount…solder *and* quick-connect terminals
- Dual primary…115/230V, 50/60 Hz
- 5 through 230V outputs; at 110mA through 35A; 25 VA through 175 VA

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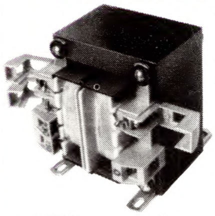

- High power, isolation/step-down transformer
- VDE certified
- UL (544 & 506) recognized and CSA certified
- Shrouded terminals…screw *and* quick-connect terminals
- Choose between 105/115/125V or 210/230/250V primary
- 115V secondary
- 300, 600, 1000 VA ratings available

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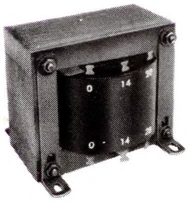

- Signal's rugged high power series
- 115V primary
- 5 through 80V output; 1 through 200A, 10 VA through 2.8 KVA
- Dual center tapped secondaries for maximum flexibility

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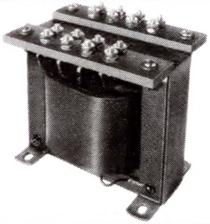

- Industrial grade stepup/stepdown
- Dual primary; 110/220V, ¼ through 10 KVA
- Available with 110/220V or 220/440V dual secondary
- Taps on primary and secondary allow ± 15% output voltage adjustment

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